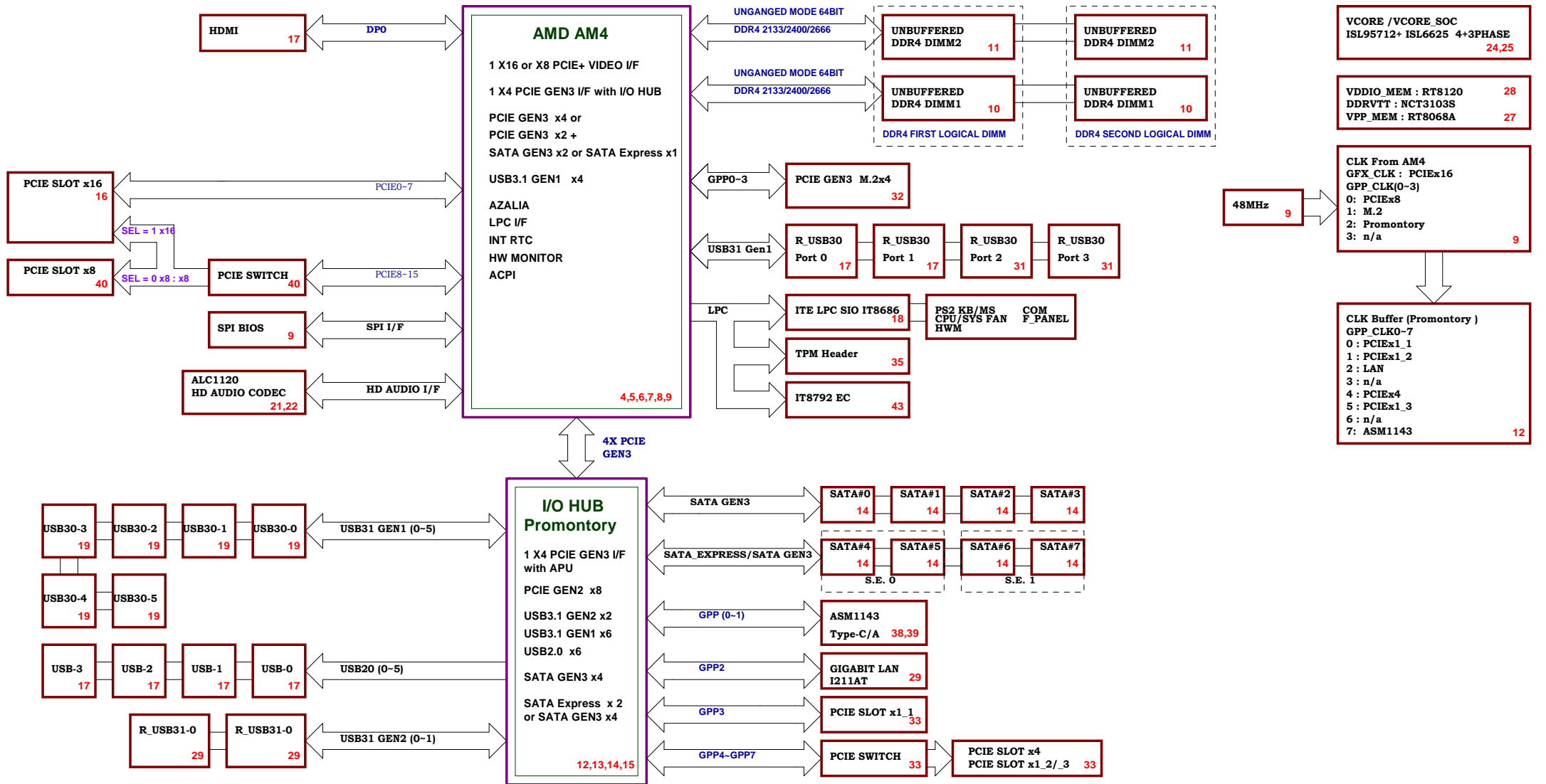


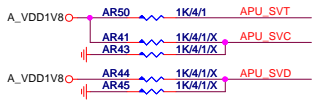
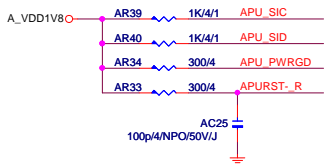
GA-AX370-Gaming K5

PAGE TITLE *Revision : 1.01*

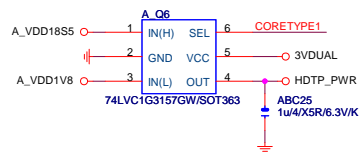
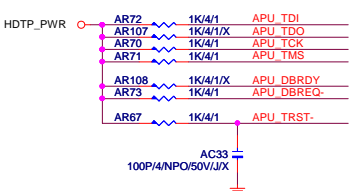
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU DDR4 MEMORY
05	CPU DDI, CONTROL
06	CPU GFX, GPP, SB, GND
07	CPU MISC
08	CPU POWER
09	CPU CLK, USB3, SPI ,LPC
10	DDR4 CHANNEL A
11	DDR4 CHANNEL B
12	PM CLK, SPI, MISC
13	PM USB
14	PM SATA, GPP
15	PM POWER & GND
16	PCI EXPRESS x16
17	HDMI, R_USB30, F_USB20
18	IT8686
19	F_USB30 ,R_USB30
20	A_VDD1V8, A_VDDPS5
21	ALC1220 CODEC
22	AUDIO JACK
23	POWER SEQ, A_VDDP
24	PWM ISL95712
25	VCORE MOS

PAGE	TITLE
26	ATX ,F_PANEL
27	PM PWR,VPP_MEM,VDDCR_SOC_S5
28	DDR POWER ,5VDUAL ,3VDUAL
29	INTEL I211AT LAN
30	PM_USB30_Redriver
31	KB_MS_USB30
32	M.2
33	PCIEx4 , PCIEx1 Slot
34	FAN
35	HWM, TPM, COM
36	CPU SMD CAP TOP
37	CPU SMD CAP BOTTOM
38	ASM1143 USB31
39	TI HD3SS3220
40	PCIEx8 Slot, SWITCH
41	CPU / AUDIO / PCIE/REAR LED
42	PCB / PCH / DDR / LED_C LED
43	IT8792 EC
44	IDT CKG 9FGL1214AKLFT

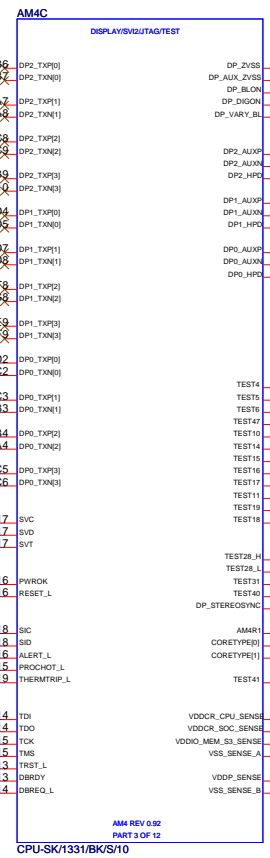
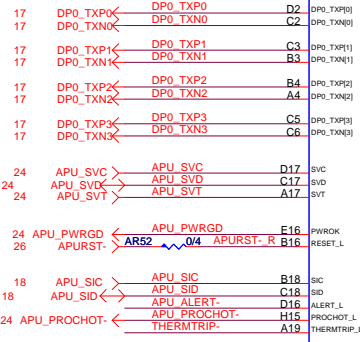




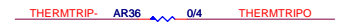
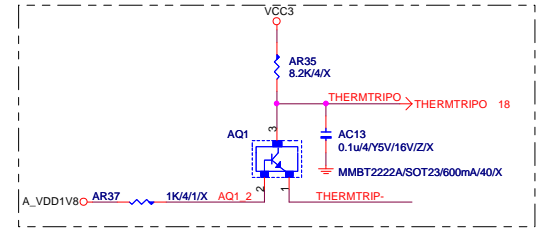
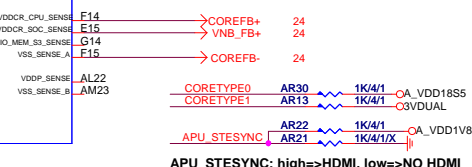
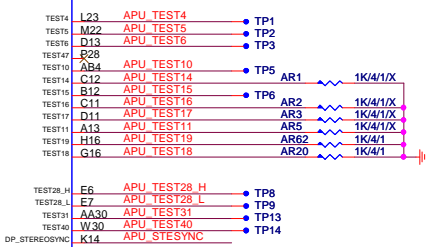
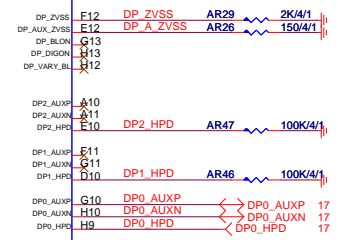
SVC	SVD	Boot voltage
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



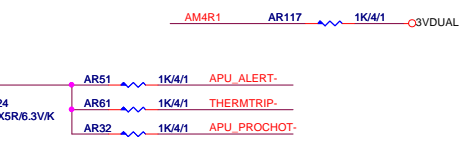
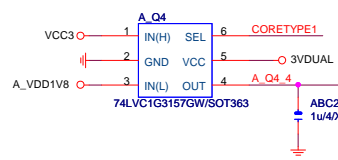
HDMI



Placed within 1500 mils from APU



APU_STESYNC: high=>HDMI, low=>NO HDMI



AM4 CPU CoreType

CORETYPE 1	CORETYPE 0	Family / Model Numbers	AM4 APU TYPE
0 BR	0	Family 15 h / Models 60 h-6 Fh	TYPE 0
0	1	Reserved	TYPE 1
1 ST	0	Family 17 h / Models 00 h-0 Fh	TYPE 2
1 RV	1	Family 17 h / Models 10 h-1 Fh	TYPE 3

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Title

CPU DDI, CONTROL

Size

Custom

Document Number

GA-AX370-Gaming K5

Rev

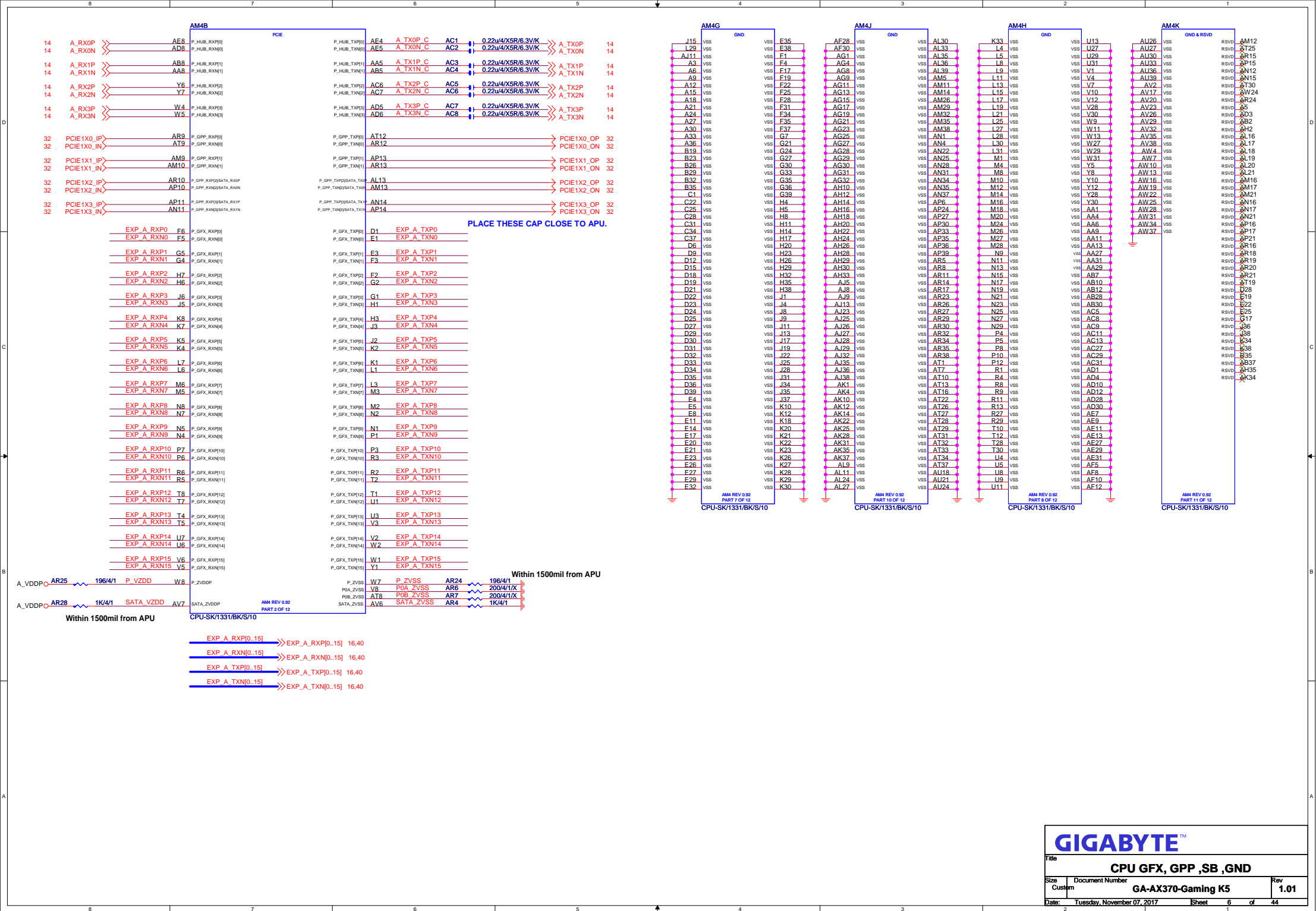
1.01

Date:

Tuesday, November 07, 2017

Sheet

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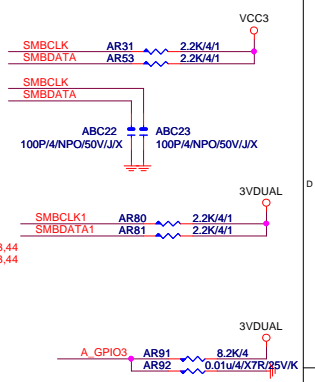
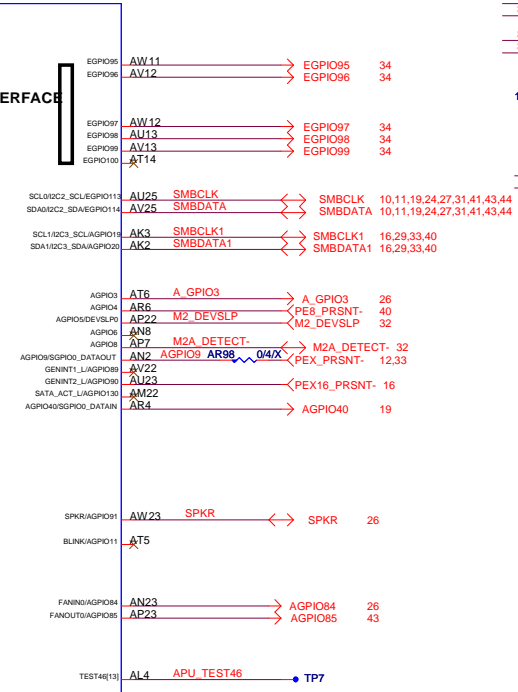
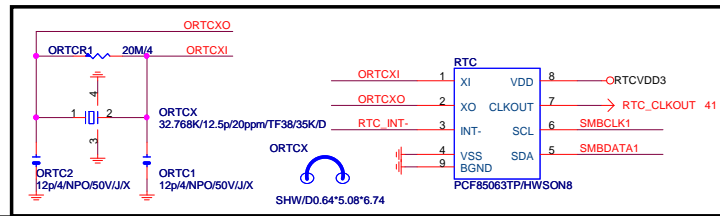
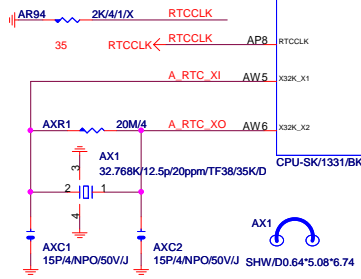
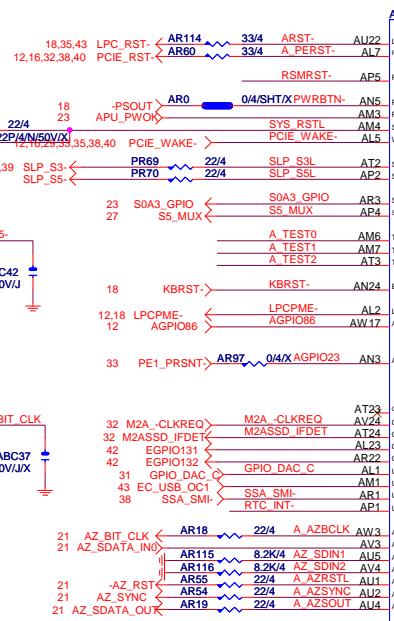
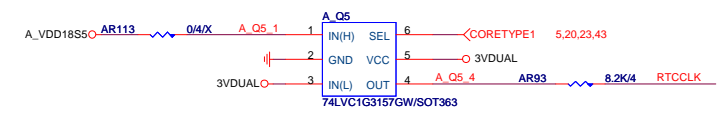
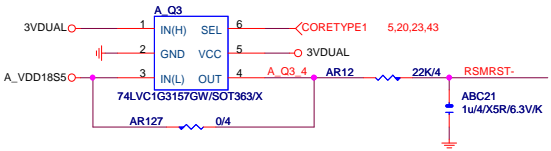
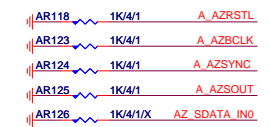
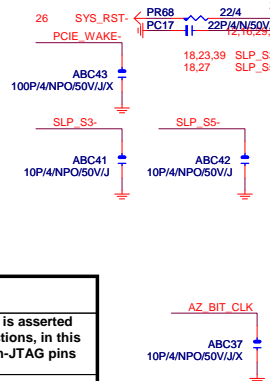


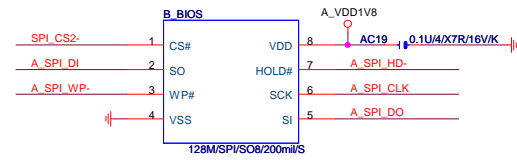
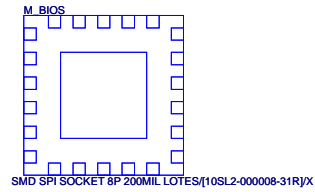
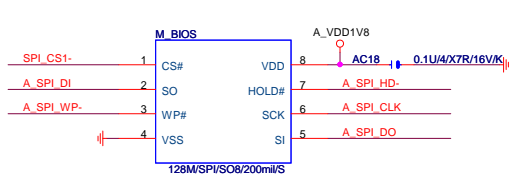
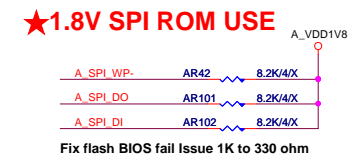
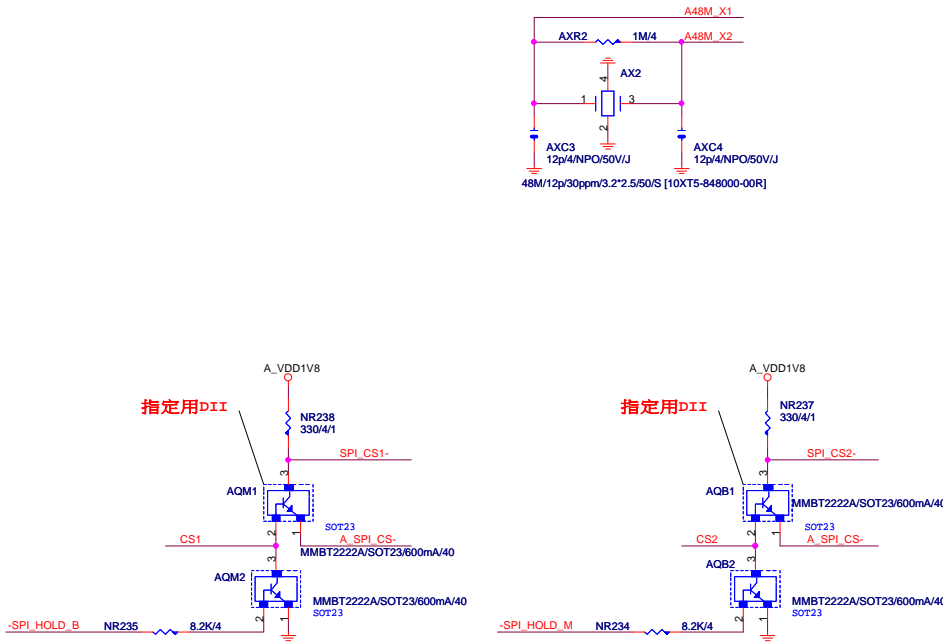
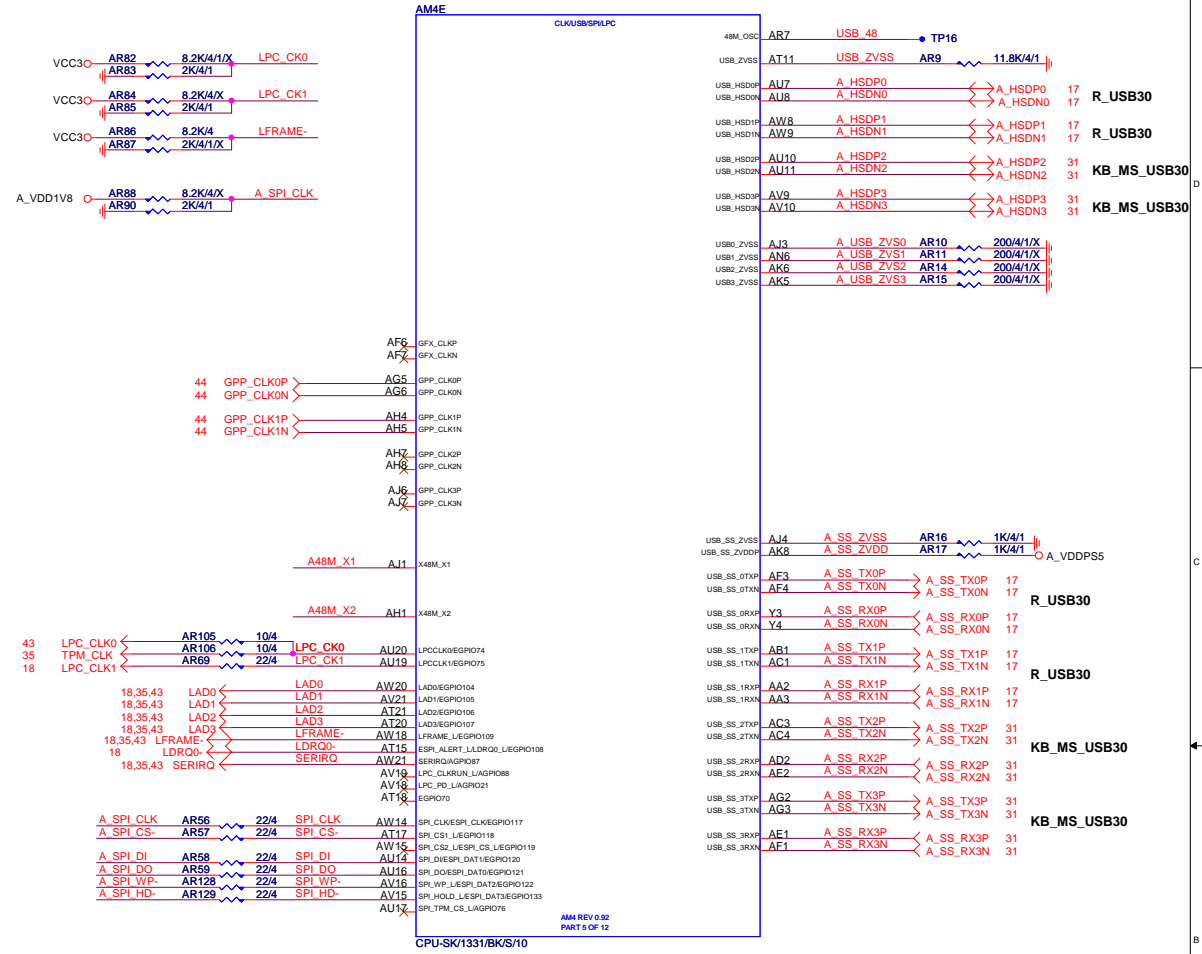
The diagram shows the following connections:

- 3VDUAL0** to **AR95** (1K/2/4/X) to **SYS_RSTL** (via a pull-up resistor)
- 3VDUAL0** to **AR96** (1K/1/1/X)
- 3VDUAL0** to **AR100** (8.2K/4/X) to **PCIE_RST-**
- VCC30** to **AR123** (8.2K/4/X)
- 3VDUAL0** to **AR104** (8.2K/4/X) to **PCIE_WAKE-**
- 3VDUAL0** to **AR112** (1K/4/1/X) to **S0A3_GPIO**
- 3VDUAL0** to **AR110** (8.2K/4/X) to **LPCPM3-**
- 3VDUAL0** to **AR111** (1K/4/1/X) to **SLP_S3-**
- 3VDUAL0** to **AR109** (1K/4/1/X) to **SLP_S5-**



TEST0	TEST1	TEST2	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAP pins overloaded for multiple functions, in this configuration the FCH JTAP are used as non-JTAG pins
0	0	1	Reserve
0	1	X	Reserve
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on JTAG only, Yuba JTAG enable.





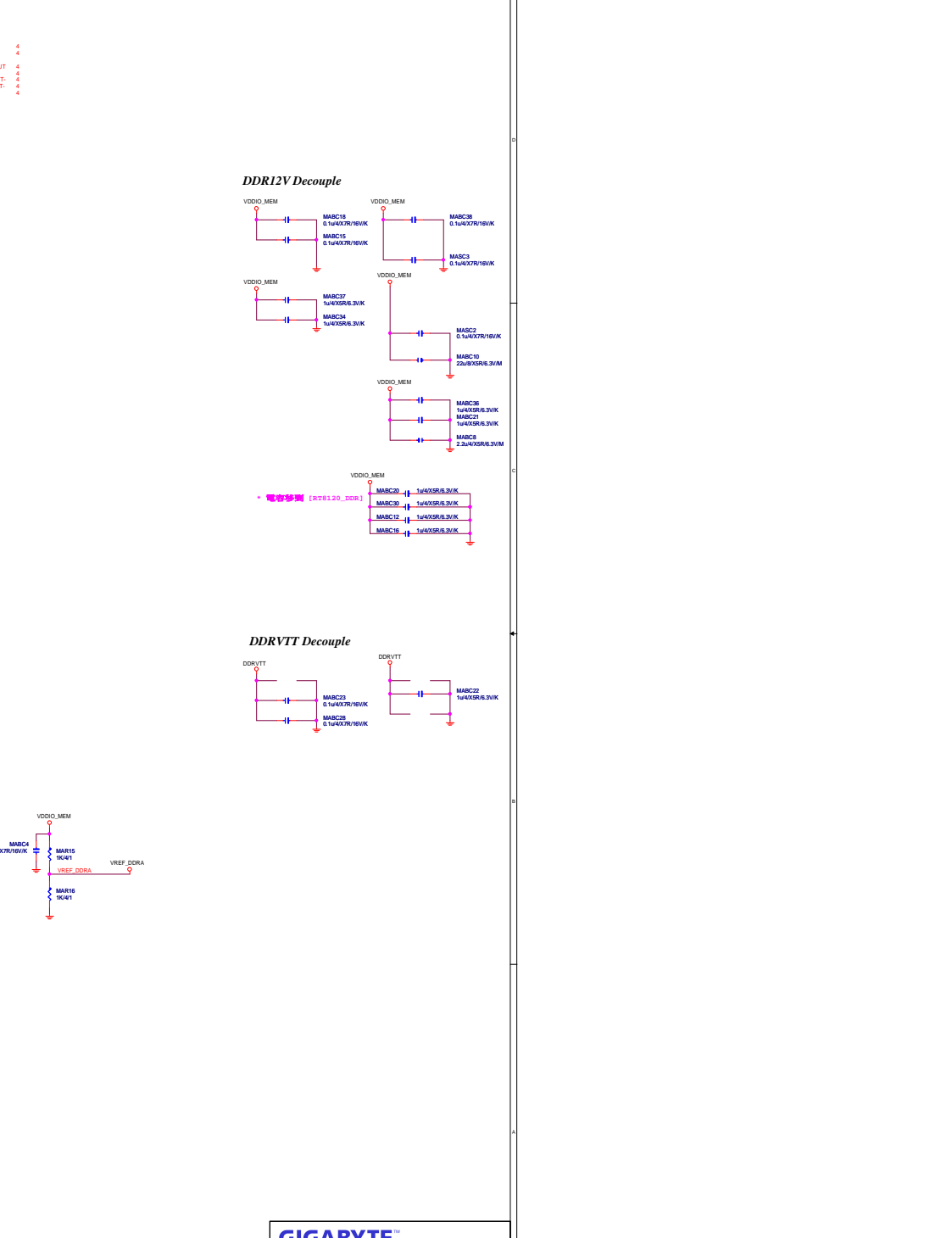
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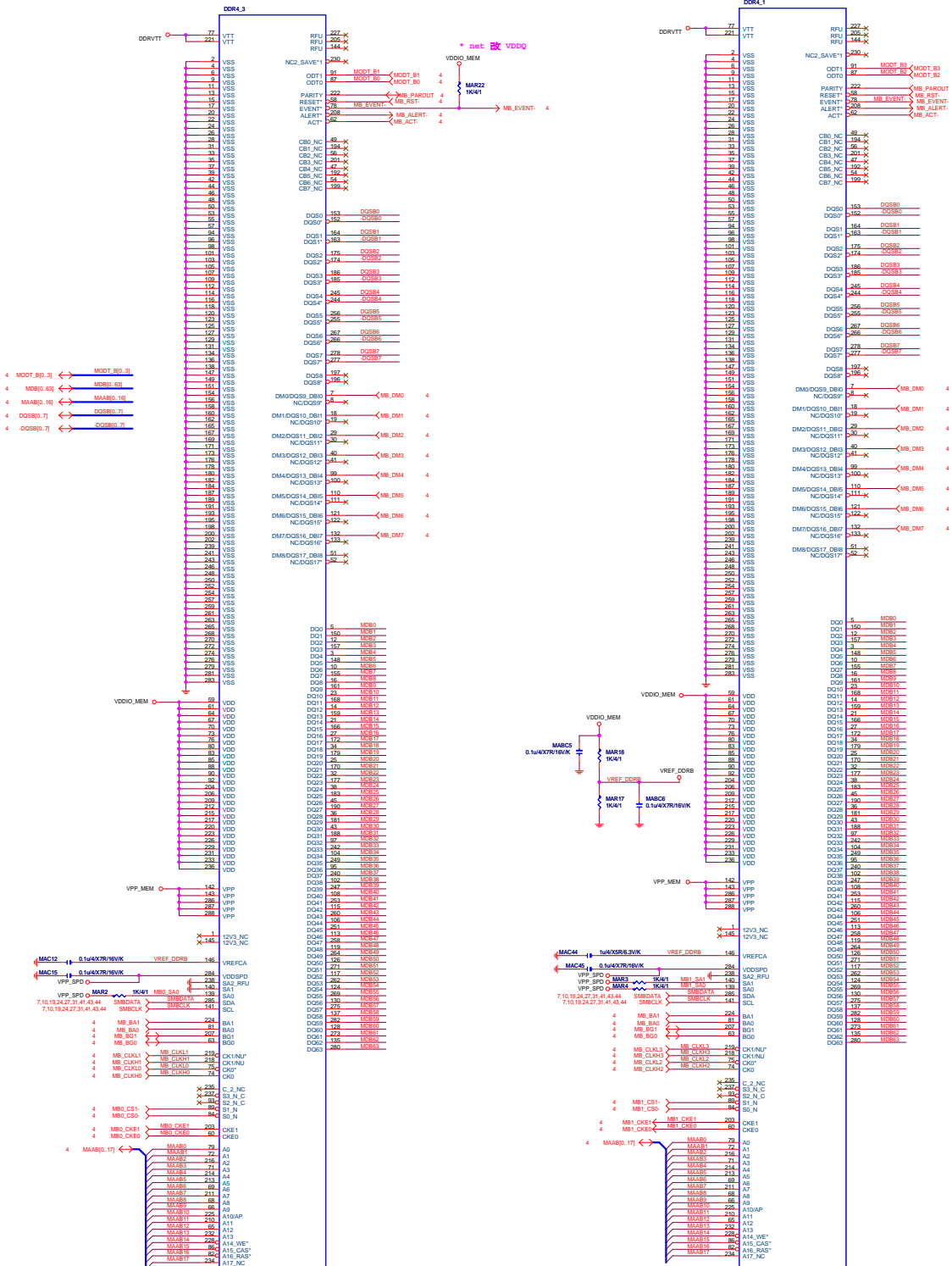
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Size: Custom Document Number: **GA-AX370-Gaming K5** Rev: **1.01**

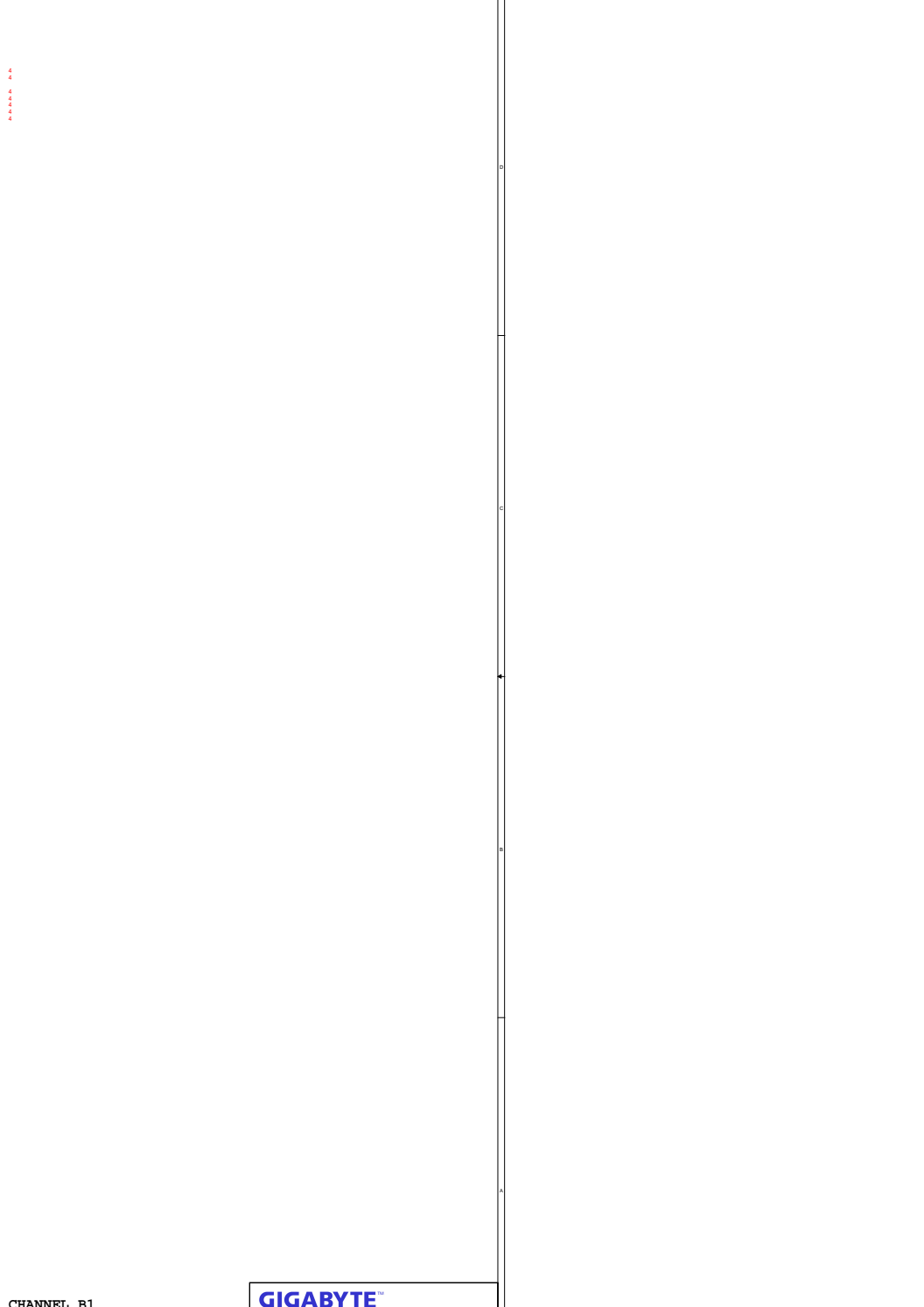
Date: Tuesday, November 07, 2017 Sheet: 9 of 44

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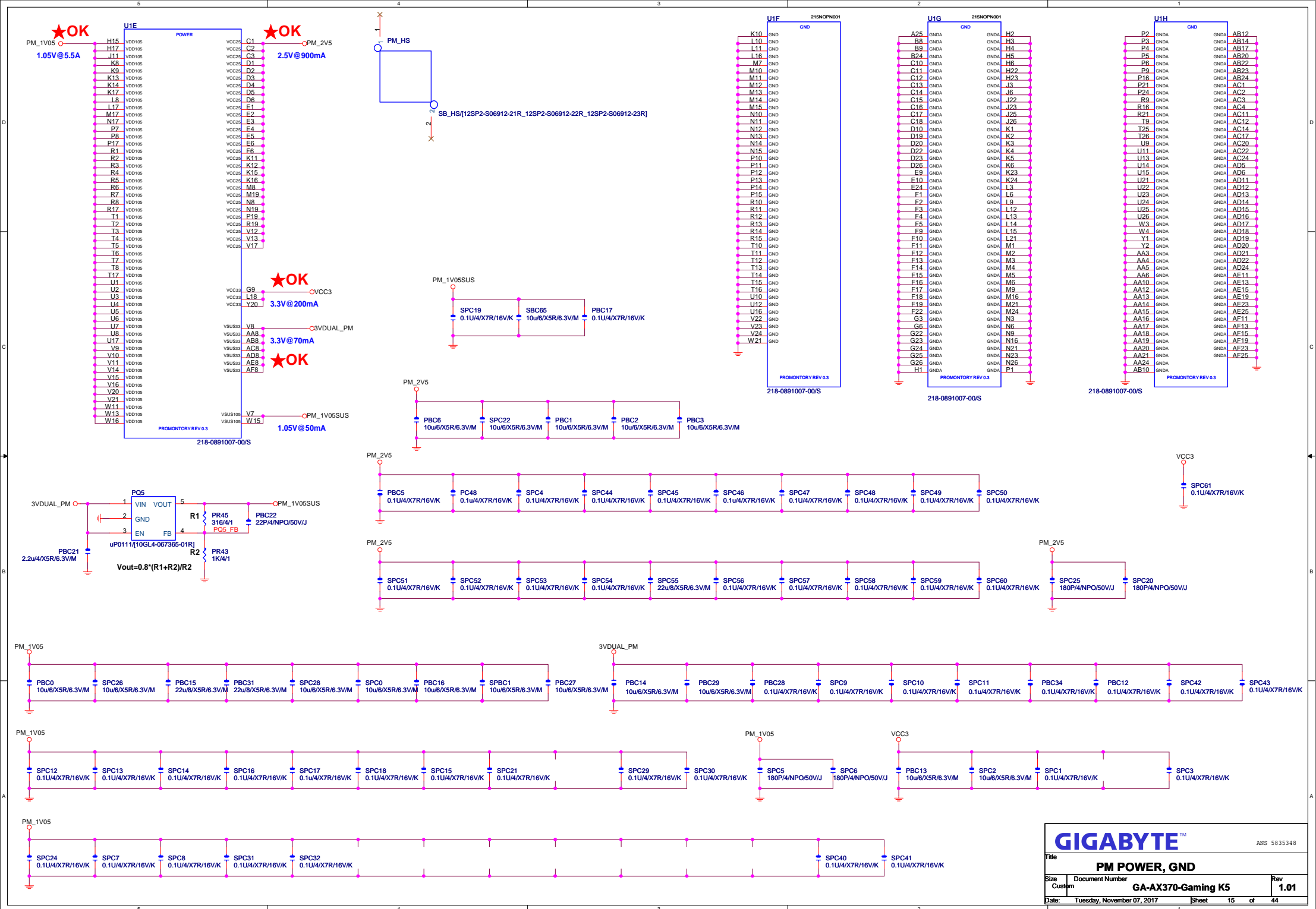


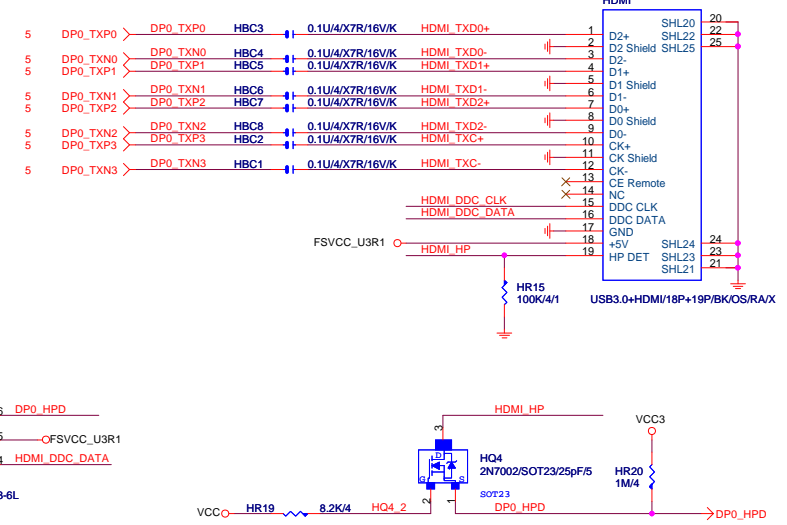
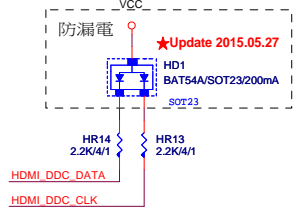
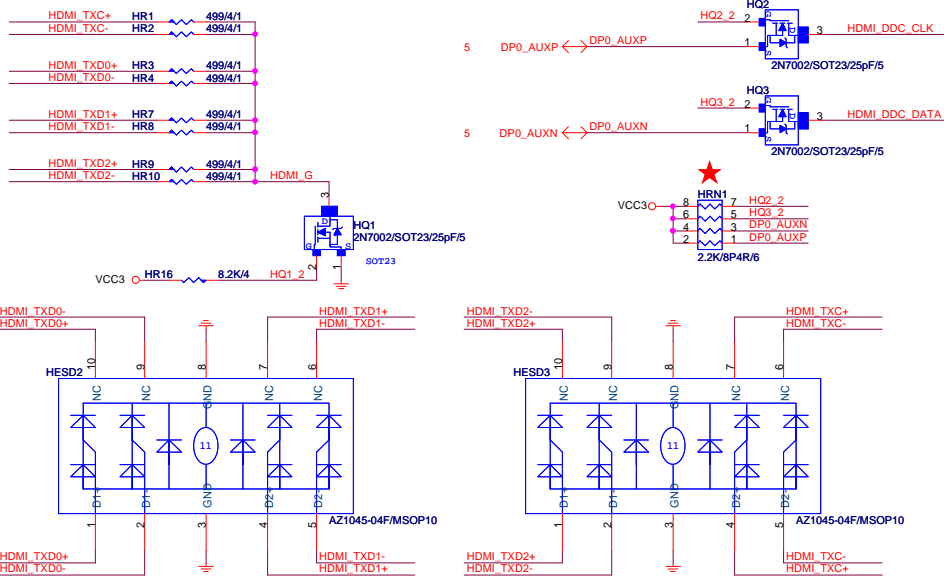


CHANNEL B0
SA2:1=001

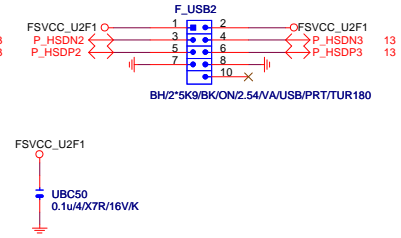


CHANNEL B1
SA2:3=011

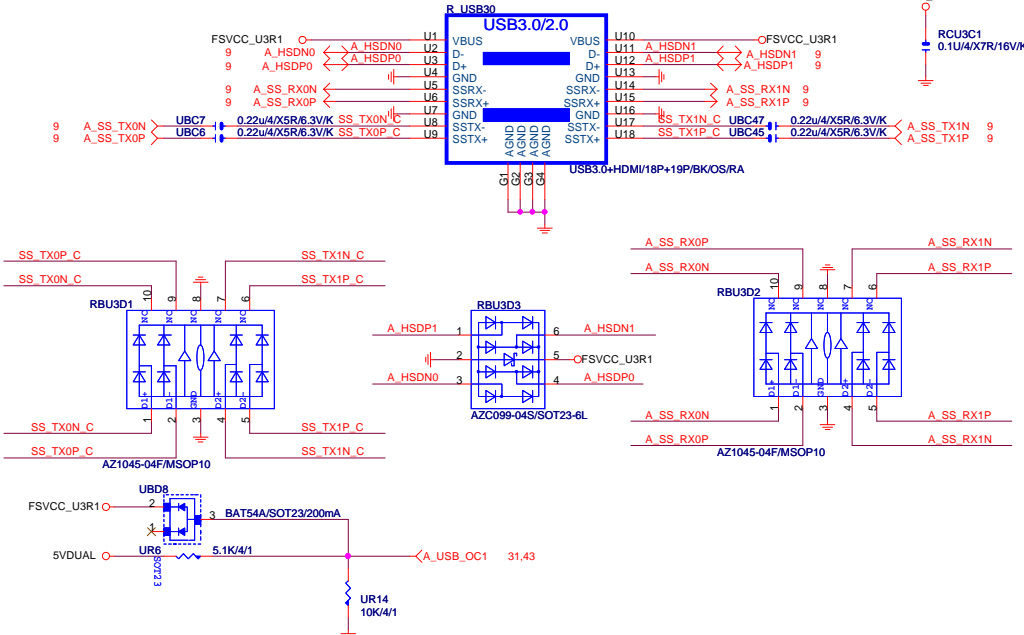
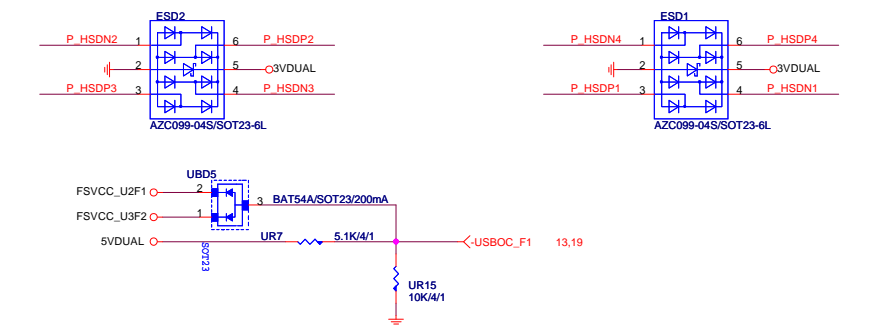
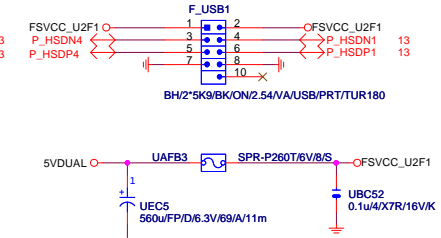




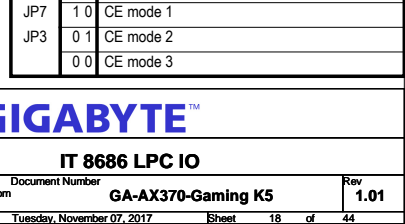
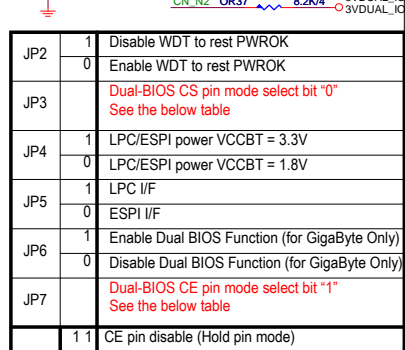
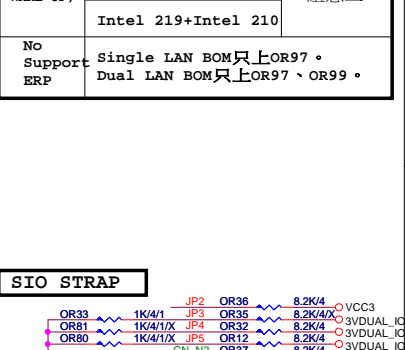
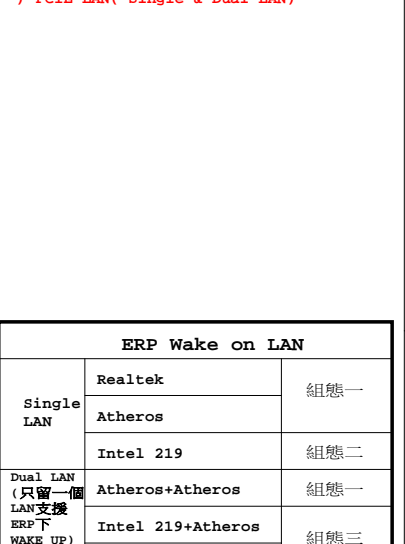
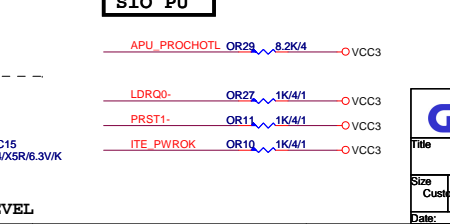
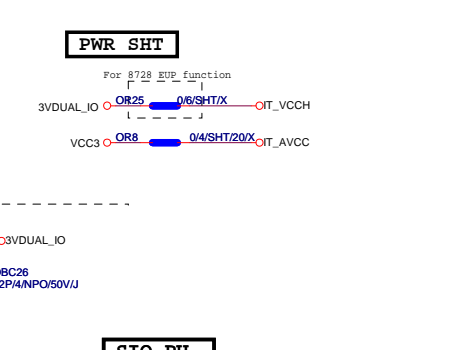
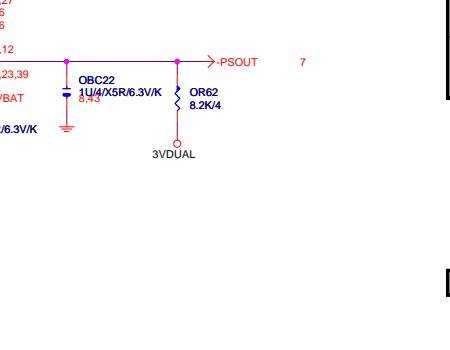
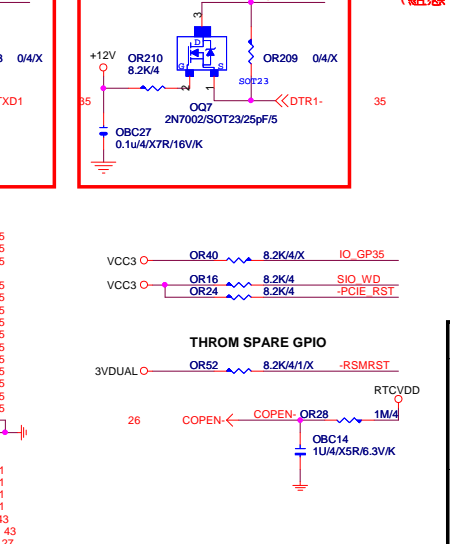
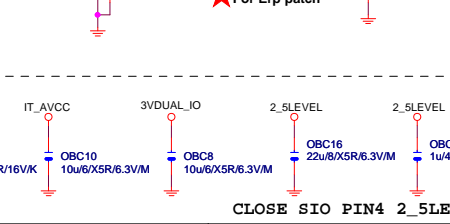
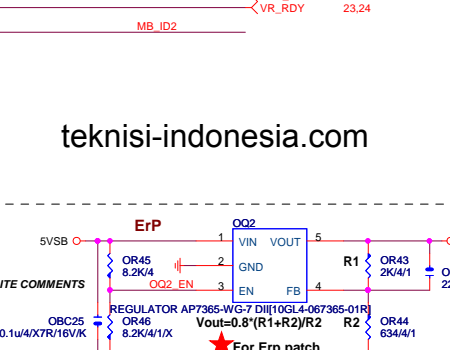
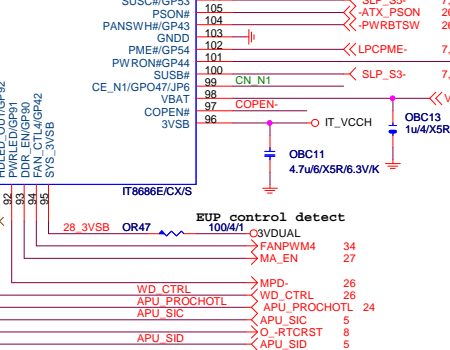
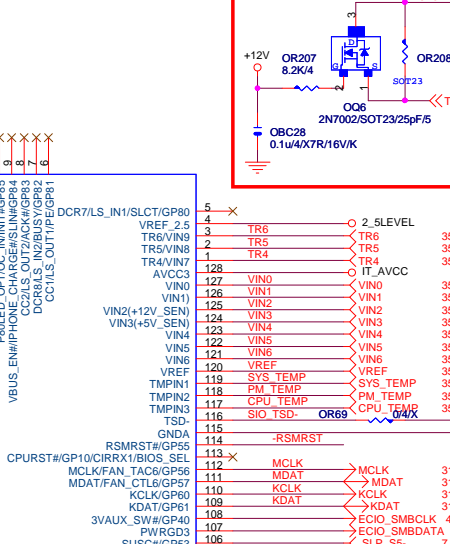
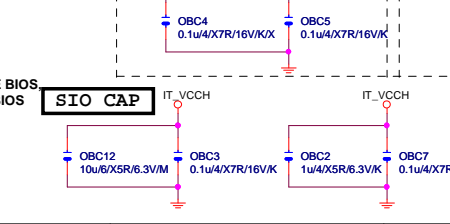
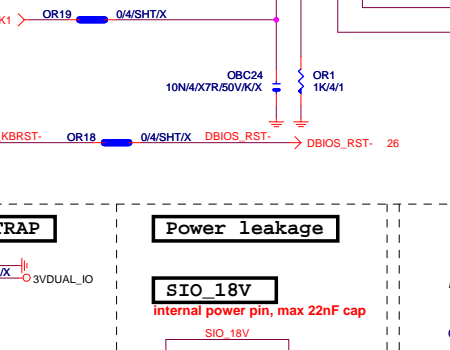
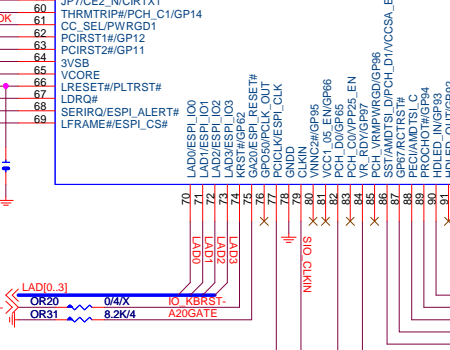
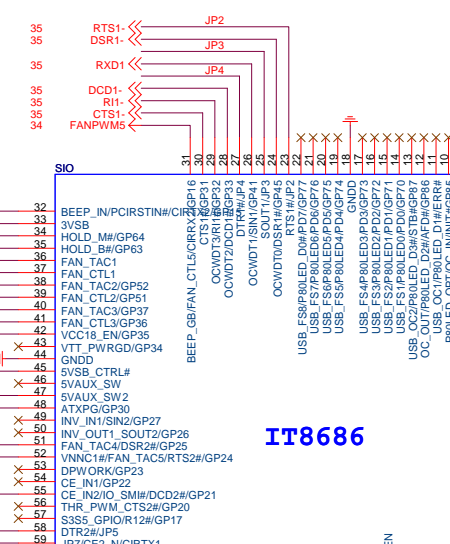
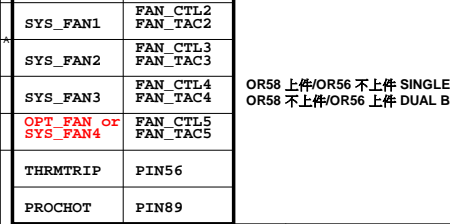
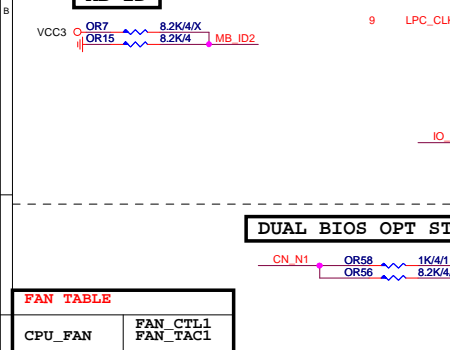
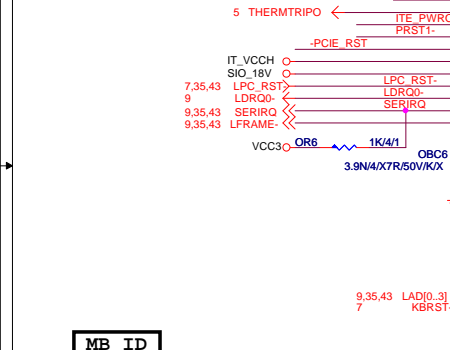
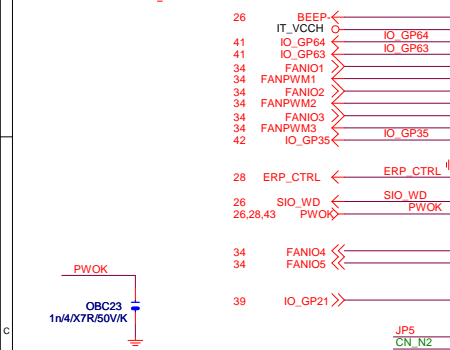
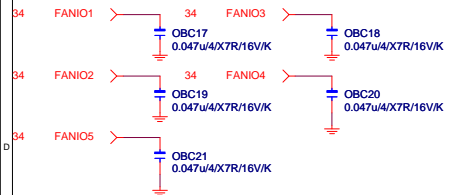
FRONT SIDE USB2



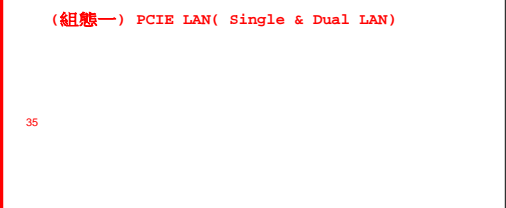
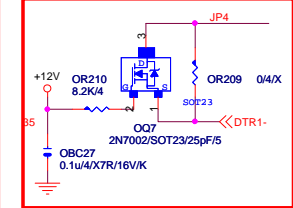
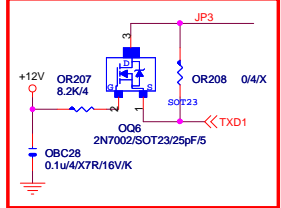
FRONT SIDE USB1



SIO IT8686 REV:0.7



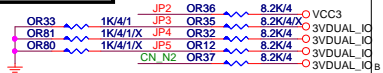
for LPC/eSPI power mode



(組態一) PCIE LAN(Single & Dual LAN)

ERP Wake on LAN		
Single LAN	Realtek	組態一
	Atheros	組態二
Dual LAN (只留一個 LAN 支援 ERP 下 WAKE UP)	Intel 219	組態一
	Atheros+Atheros	組態二
	Intel 219+Atheros	組態三
No Support ERP	Single LAN BOM 只上 OR97	
	Dual LAN BOM 只上 OR97、OR99	

SIO STRAP



JP2	1	Disable WDT to rest PWROK
JP2	0	Enable WDT to rest PWROK
JP3	1	Dual-BIOS CS pin mode select bit "0"
JP3	0	See the below table
JP4	1	LPC/ESPI power VCCBT = 3.3V
JP4	0	LPC/ESPI power VCCBT = 1.8V
JP5	1	LPC I/F
JP5	0	ESPI I/F
JP6	1	Enable Dual BIOS Function (for GigaByte Only)
JP6	0	Disable Dual BIOS Function (for GigaByte Only)
JP7	1	Dual-BIOS CE pin mode select bit "1"
JP7	0	See the below table
JP7	1 1	CE pin disable (Hold pin mode)
JP7	1 0	CE mode 1
JP3	0 1	CE mode 2
JP3	0 0	CE mode 3

GIGABYTE™

IT 8686 LPC IO

Title

Document Number

Rev

GA-AX370-Gaming K5

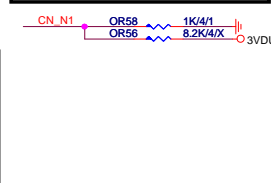
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Tuesday, November 07, 2017

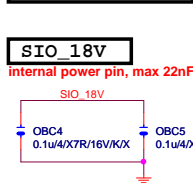
Sheet 18 of 44

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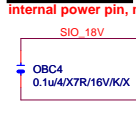
DUAL BIOS OPT STRAP



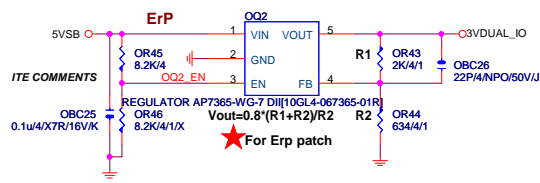
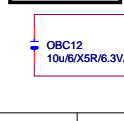
Power leakage



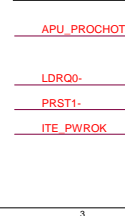
SIO 18V



SIO CAP

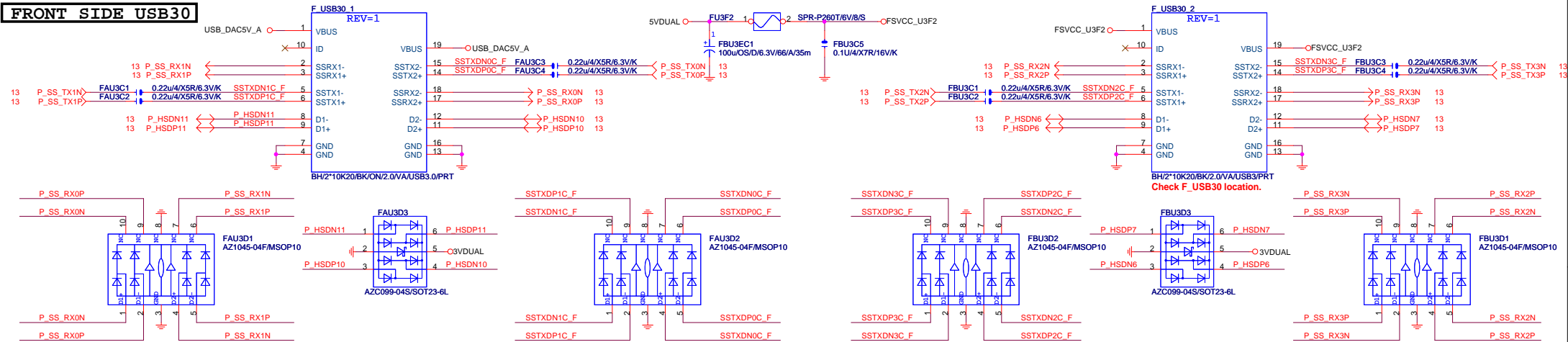


SIO PU

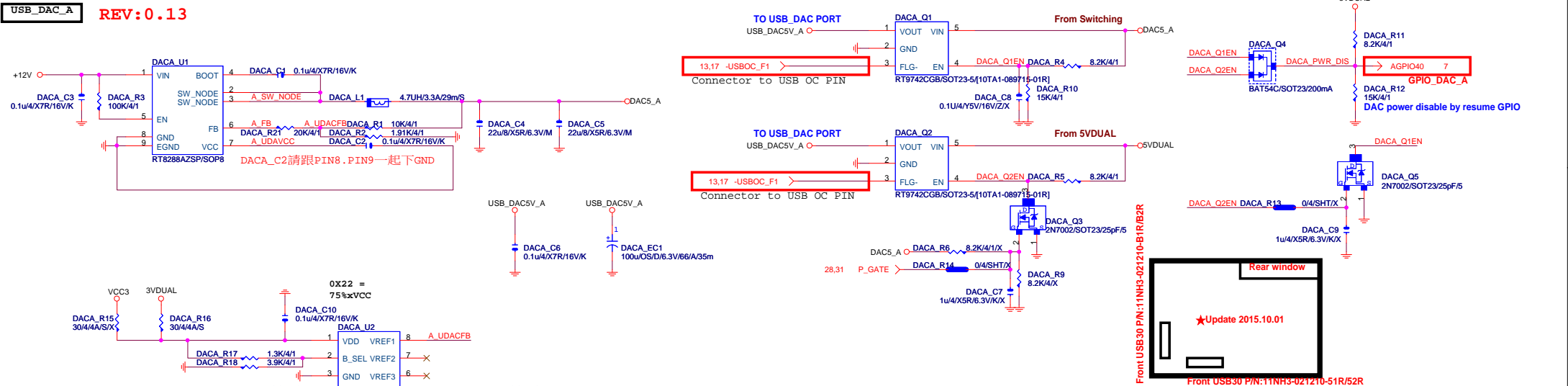


CLOSE SIO PIN4 2_5LEVEL

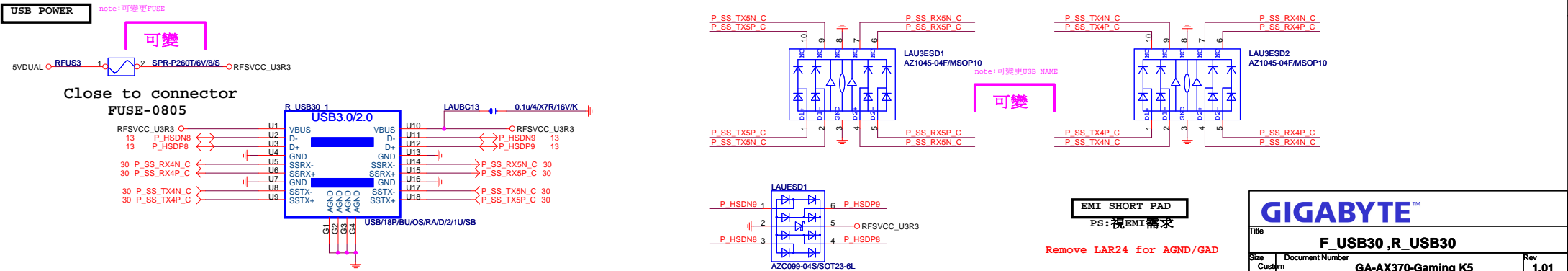
FRONT SIDE USB30



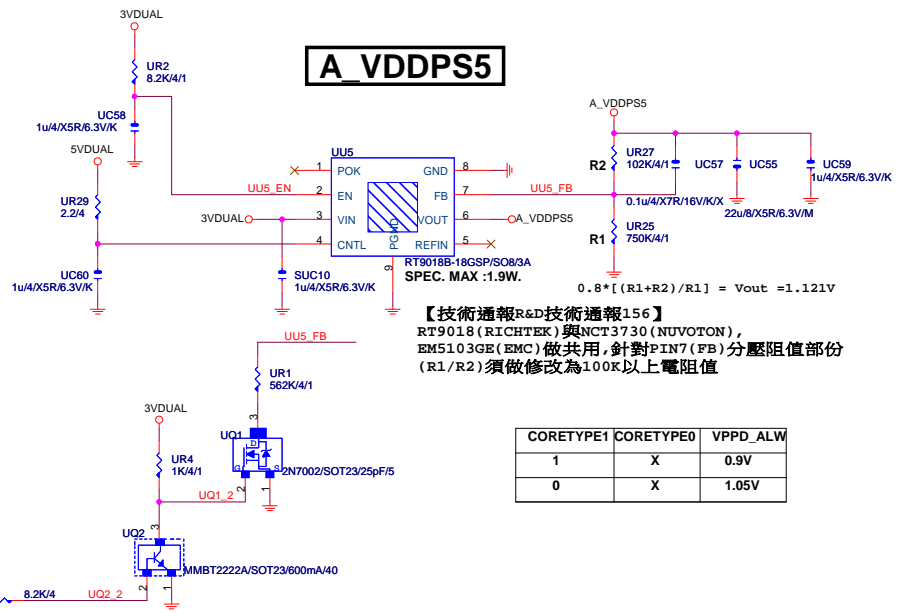
USB_DAC_A REV:0.13



USB POWER note:可變更FUSE



A_VDDPS5

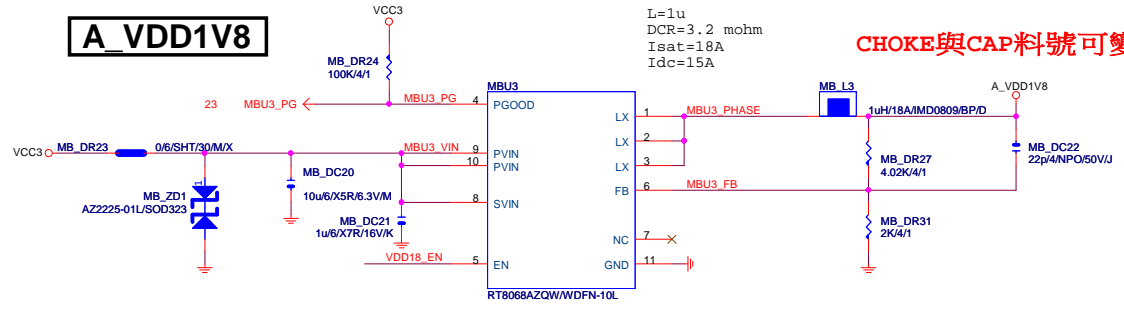


【技術通報R&D技術通報156】
RT9018 (RICHTER) 與 NCT3730 (NUVOTON),
EM5103GE (EMC) 做共用, 針對 PIN7 (FB) 分壓阻值部份
(R1/R2) 須做修改為 100K 以上電阻值

CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V

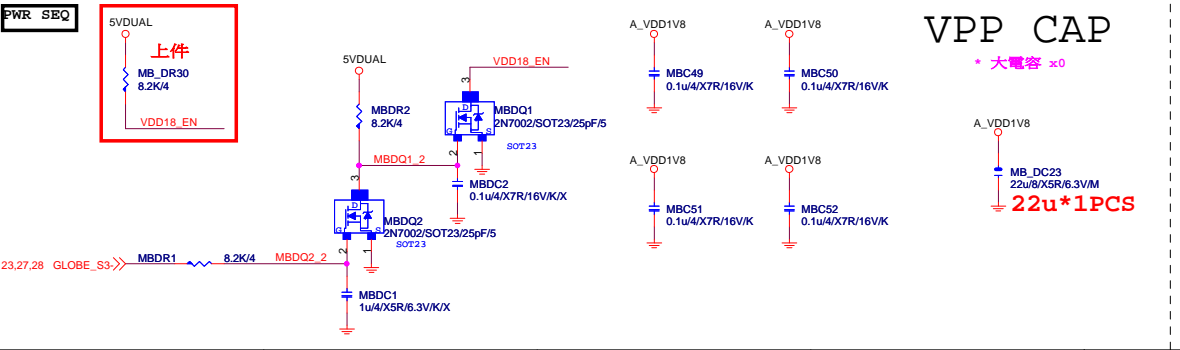
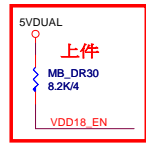
REV:0.4

A_VDD1V8



CHOKE與CAP料號可變

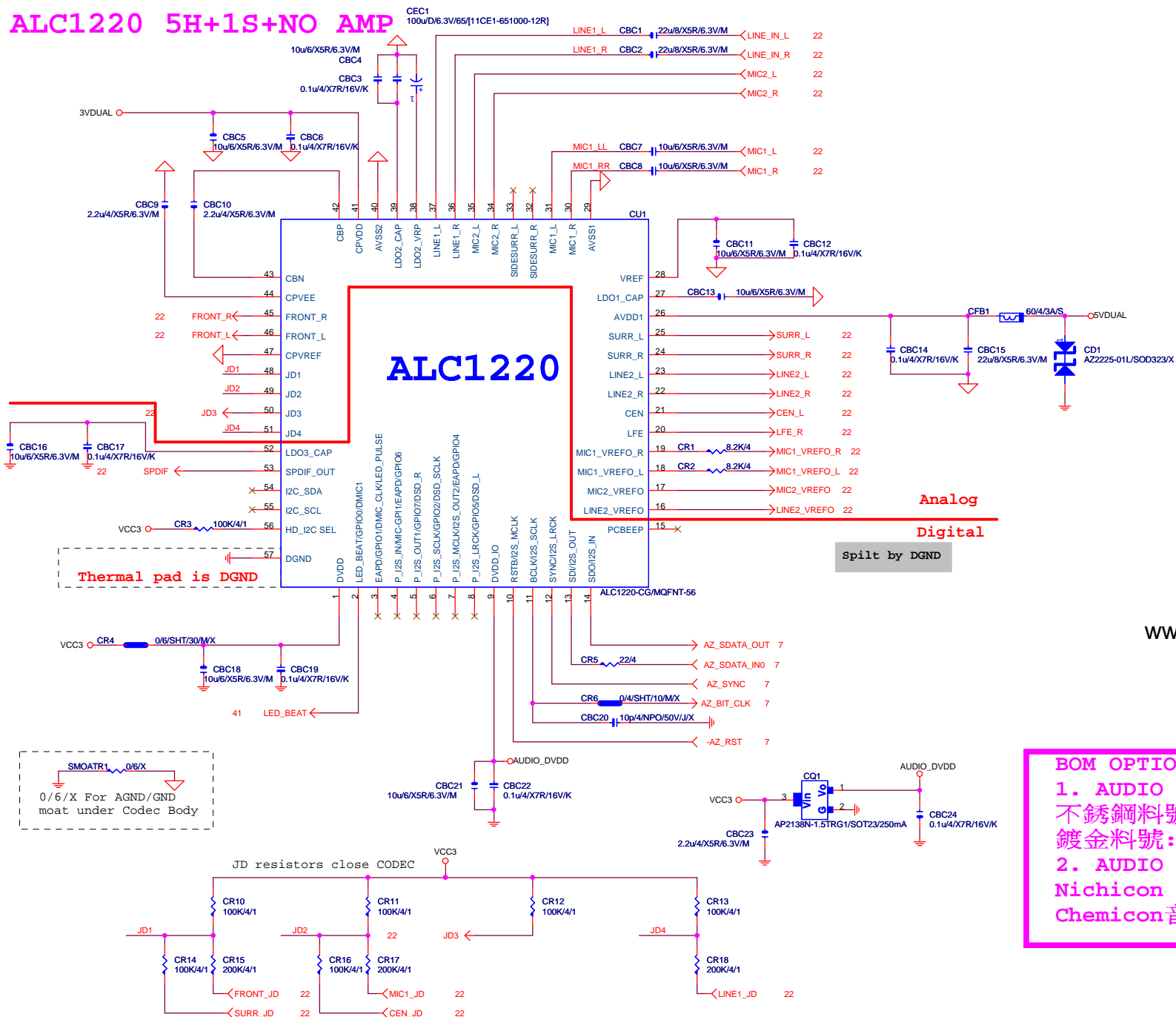
PWR SEQ



VPP CAP

* 大電容 >= 0.22uF
22u*1PCS

ALC1220 5H+1S+NO AMP



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BOM OPTION :

1. AUDIO CONNECT

不銹鋼料號:11NR6-403025-A3R

鍍金料號:11NR6-403025-92R

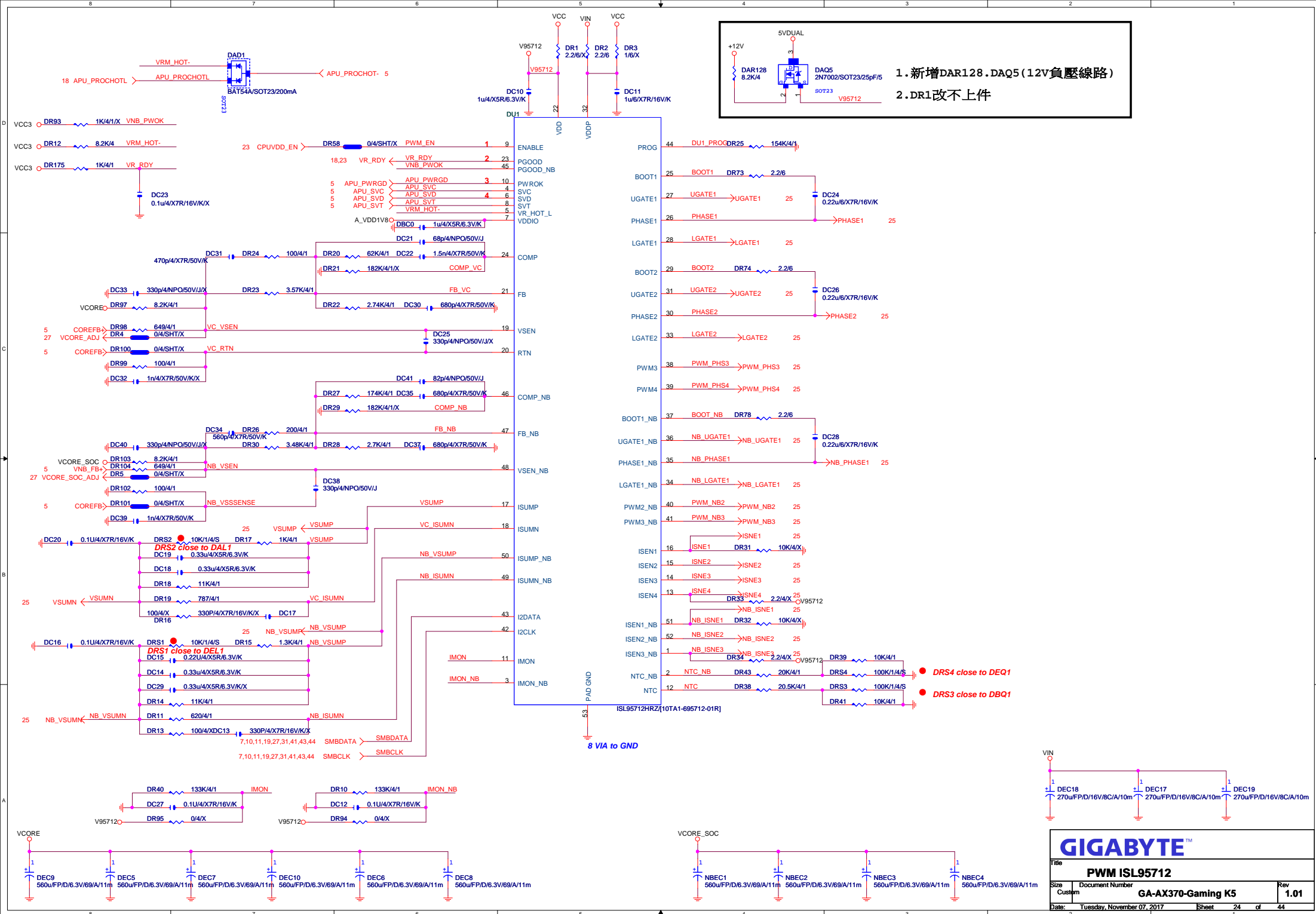
2. AUDIO CAP

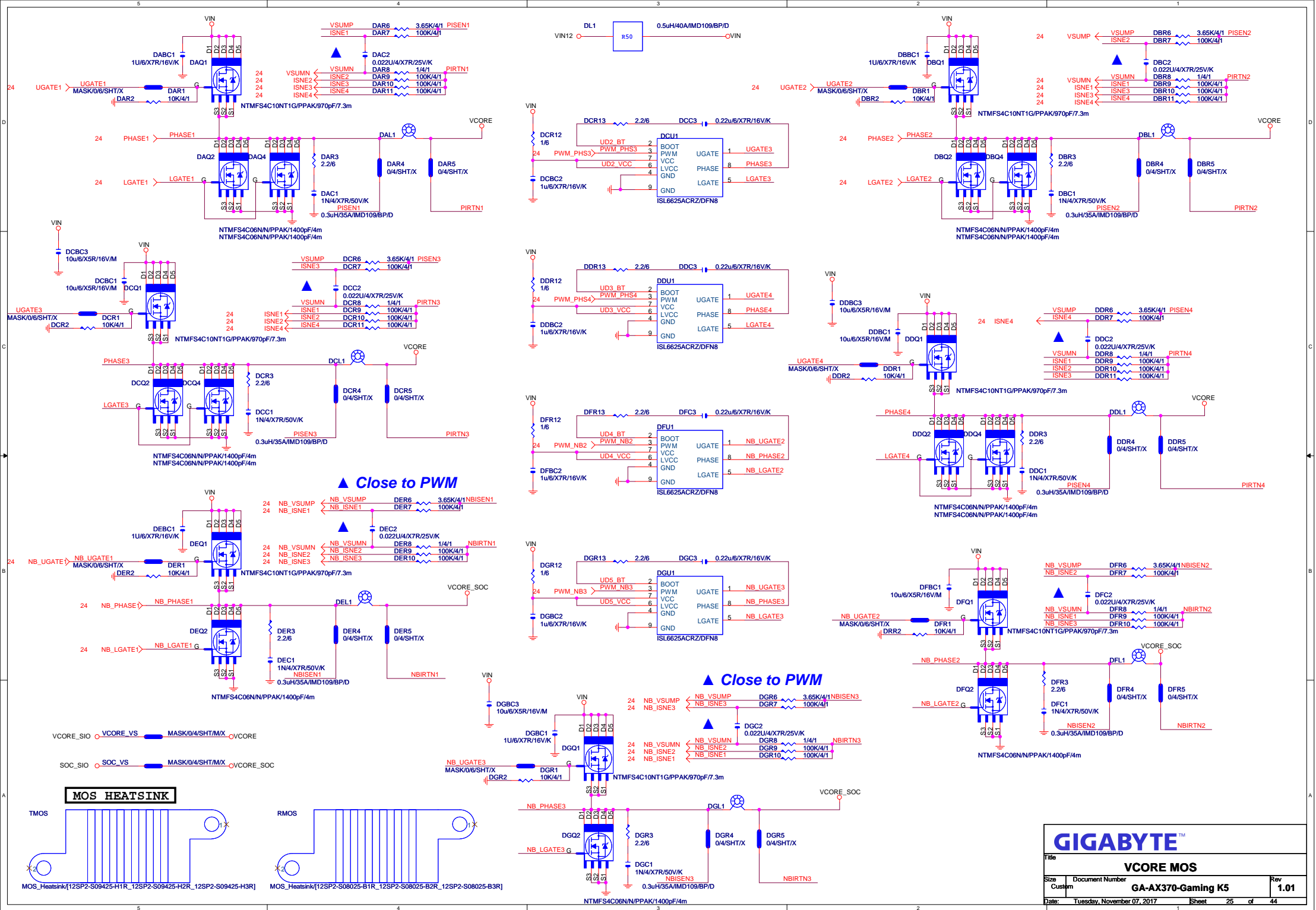
Nichicon MW音效電容 : 11CE1-651000-12R

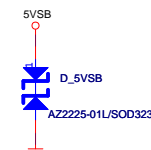
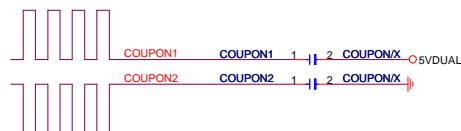
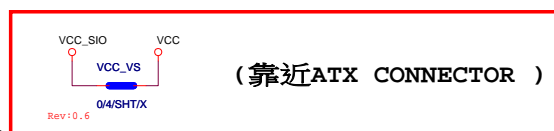
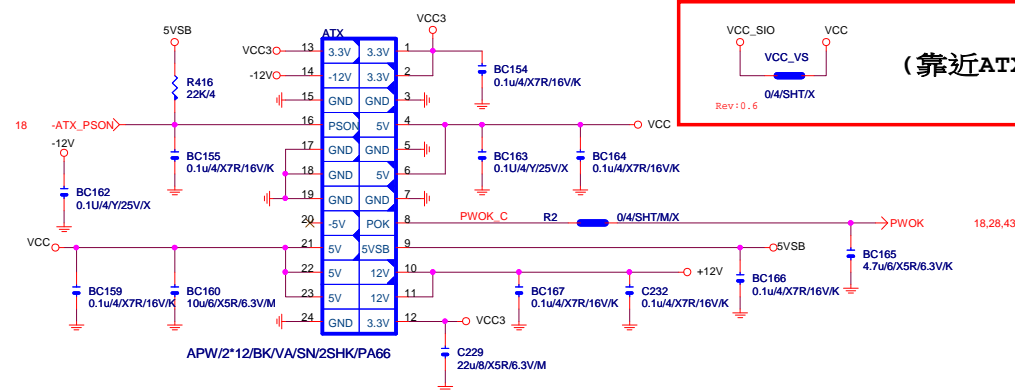
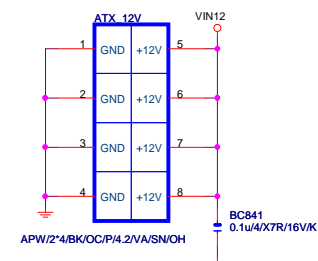
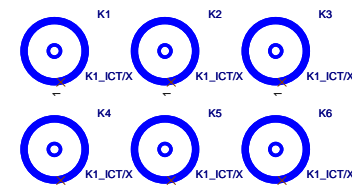
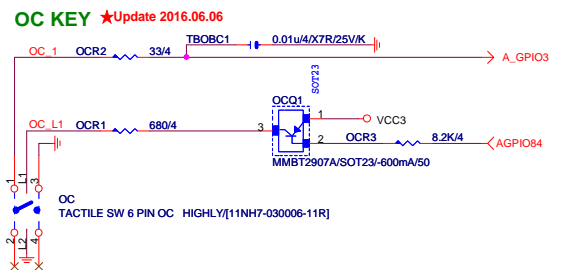
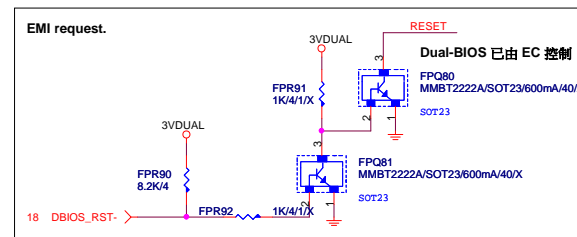
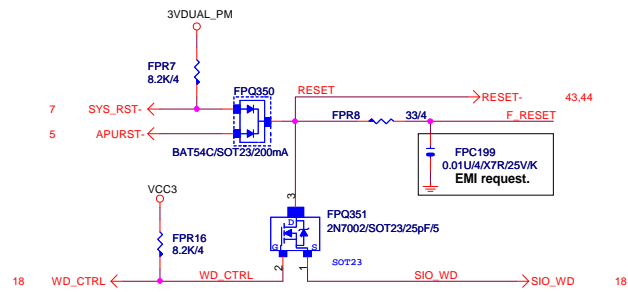
Chemicon音效電容 : 11CE2-651000-05R

Gigabyte Technology

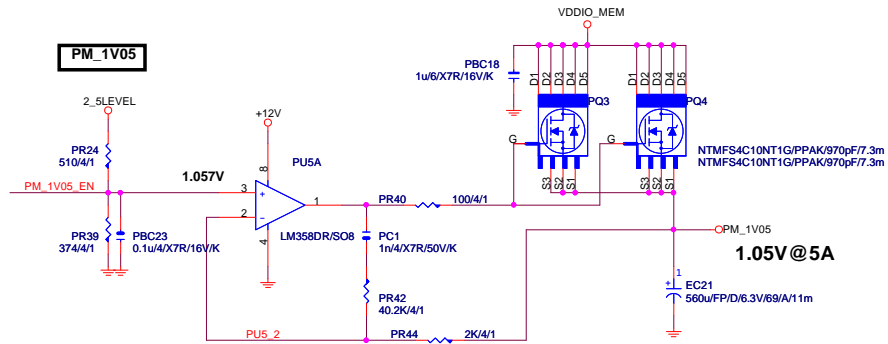
Title	ALC1220		
Size	Document Number	Rev	
Custom	GA-AX370-Gaming K5	1.01	
Date:	Tuesday, November 07, 2017	Sheet	21 of 44



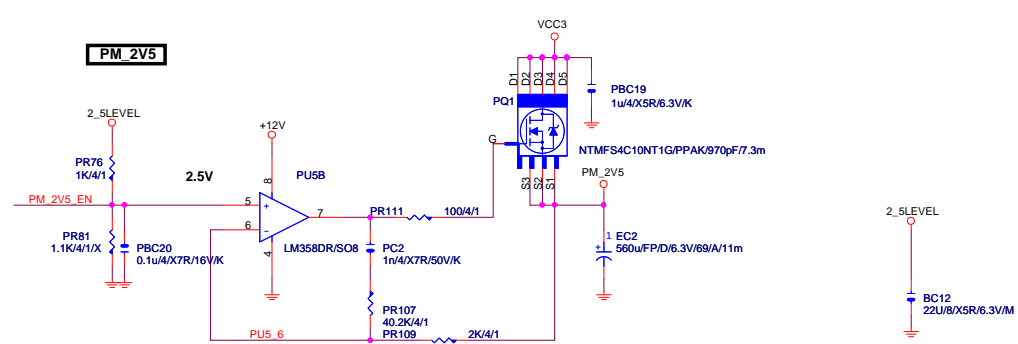




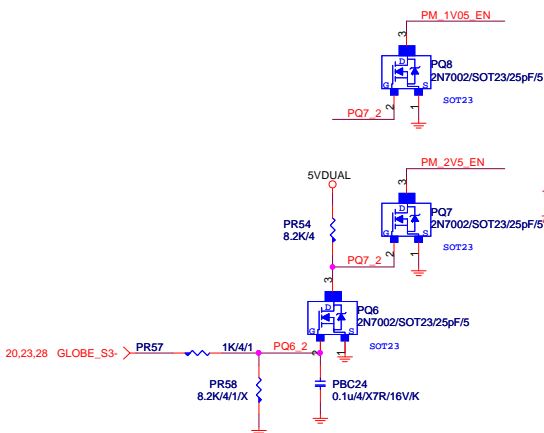
PM_1V05



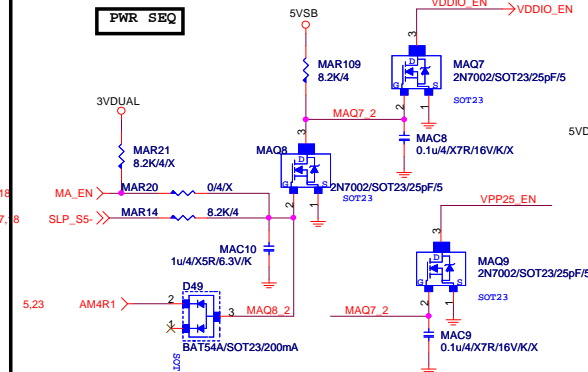
PM_2V5



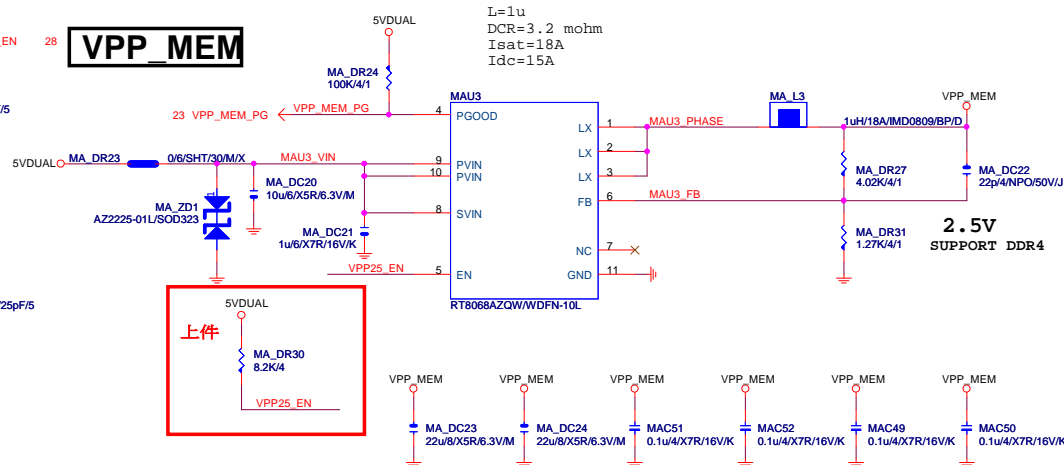
PWR_SEQ



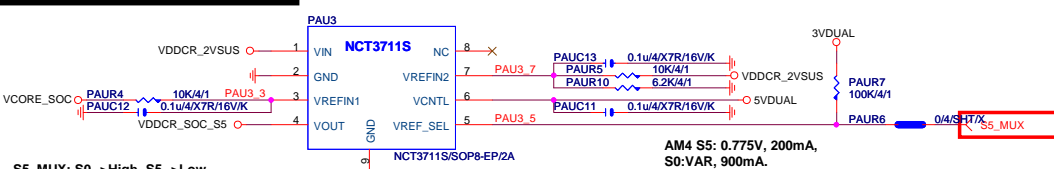
PWR_SEQ



VPP_MEM



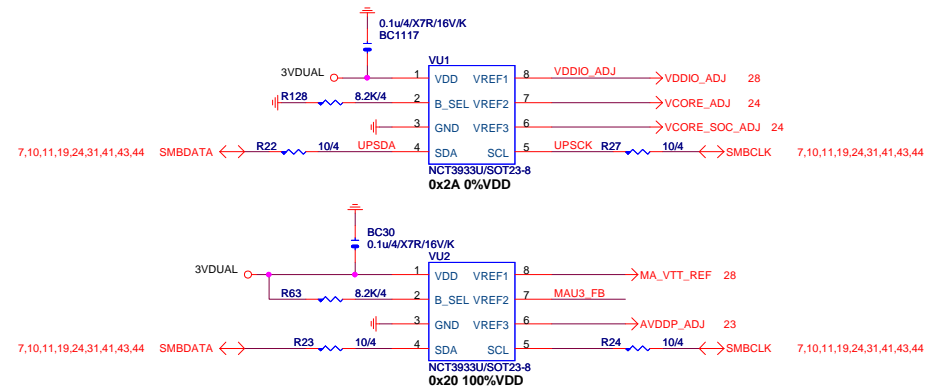
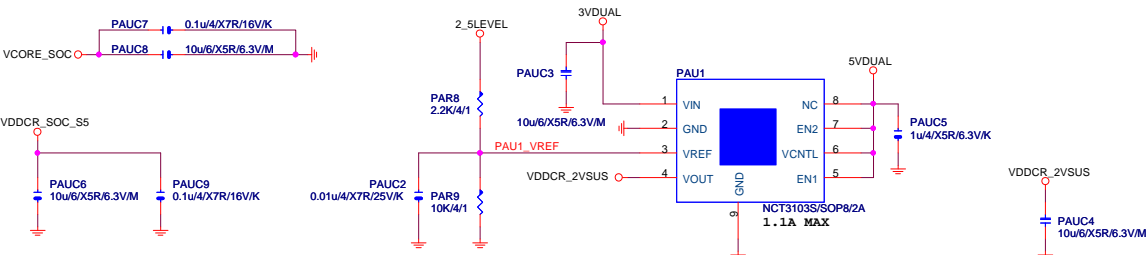
VDDCR SOC S5



S5_MUX: S0-->High, S5-->Low

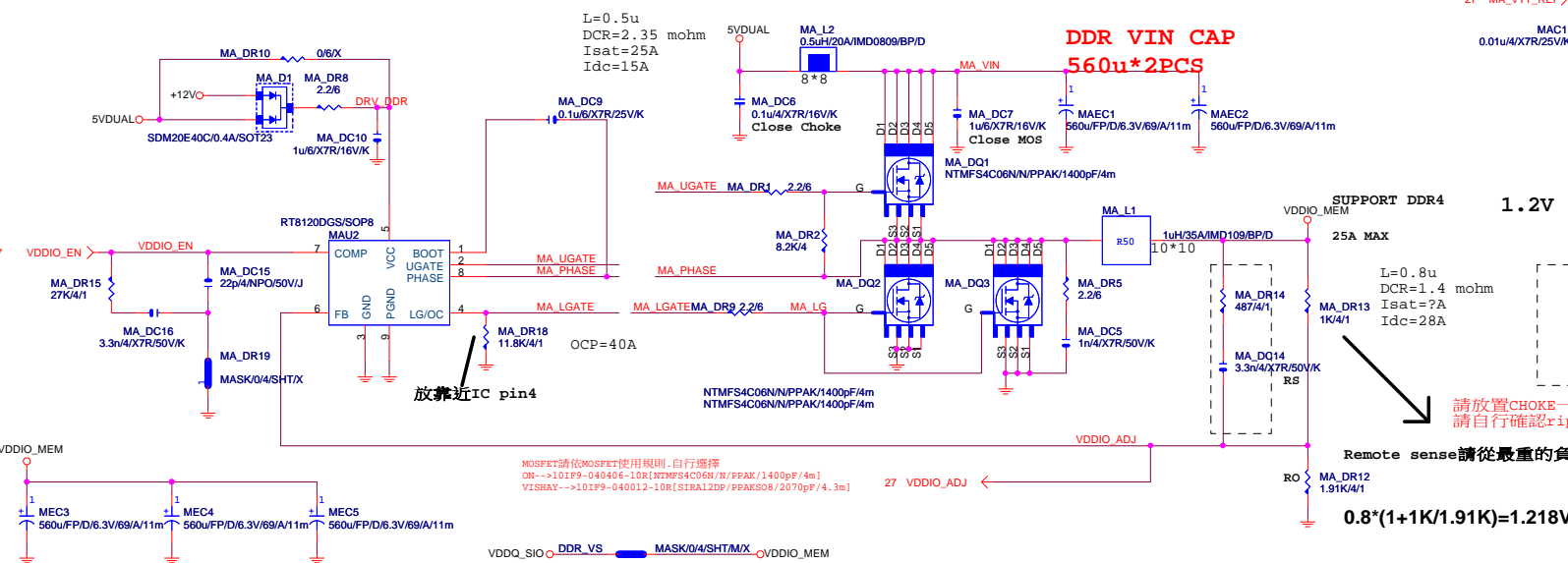
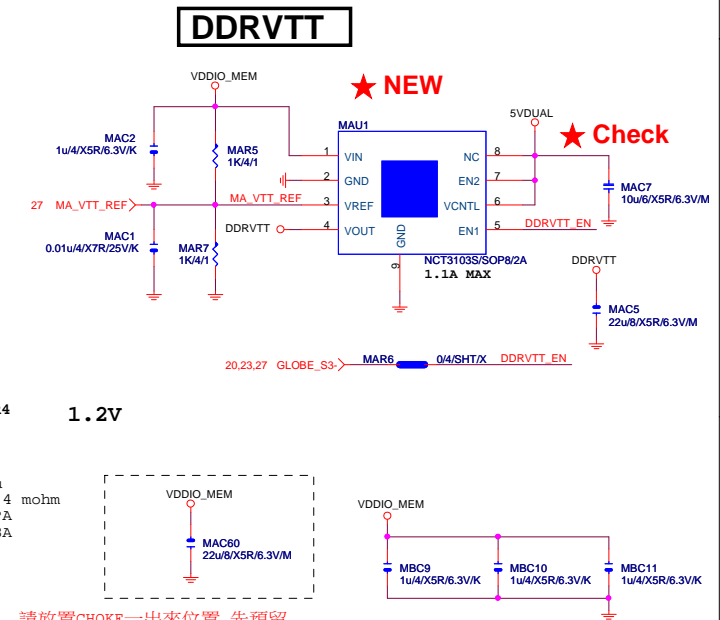
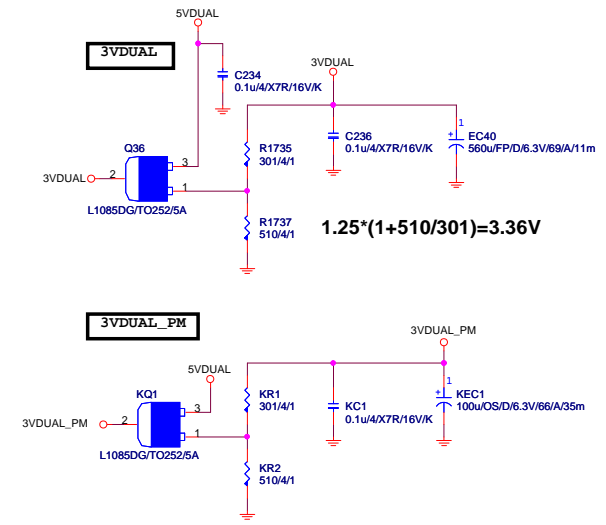
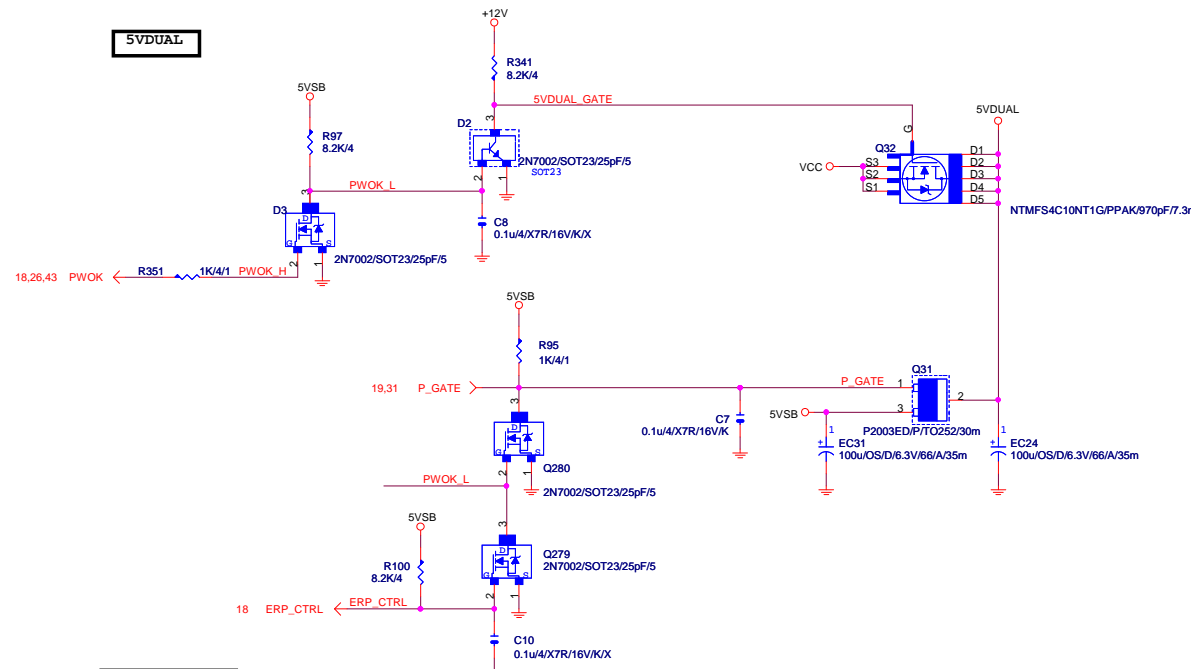
H: VDDCR_SOC_S5 will track VCORE_SOC.

L: If VCORE_SOC < 0.775V (OR 0.85V), VDDCR_SOC_S5=0.775V.
If VCORE_SOC >= 0.775V (OR 0.85V), VDDCR_SOC_S5 will track VCORE_SOC.



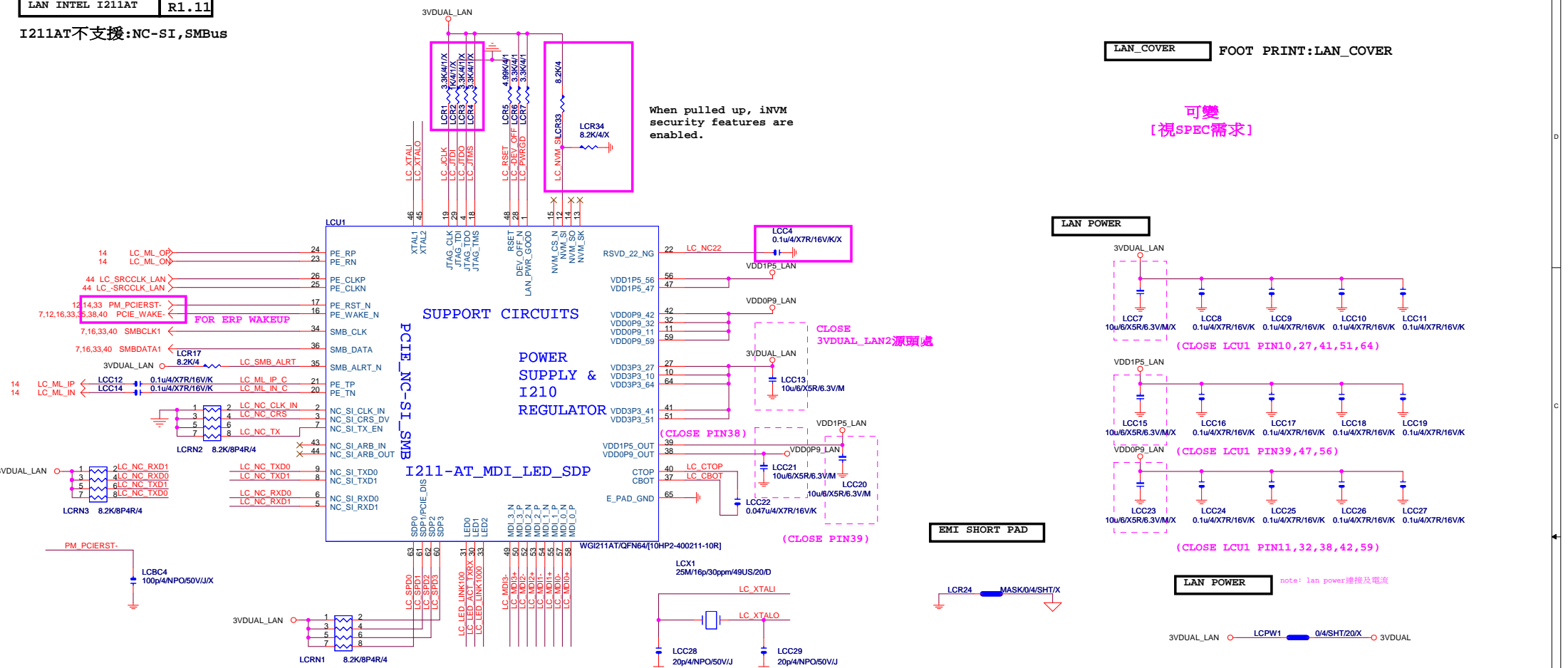
GIGABYTE

Title		
PM PWR,VPP_MEM,VDDCR_SOC_S5		
Size	Document Number	Rev
Custom	GA-AX370-Gaming K5	1.01
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Title			
DDR POWER, 5VDUAL, 3VDUAL			
Size	Document Number	Rev	
Custom	GA-AX370-Gaming K5	1.01	
Date:	Tuesday, November 07, 2017	Sheet	28 of 44

可變
[視SPEC需求]

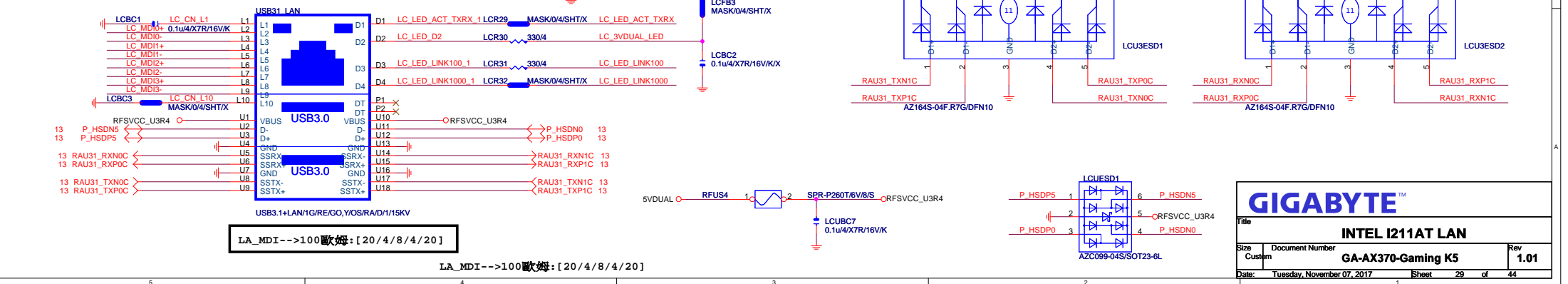


USB LAN

USB LAN CONNECTOR

note:可變更 USB NAME

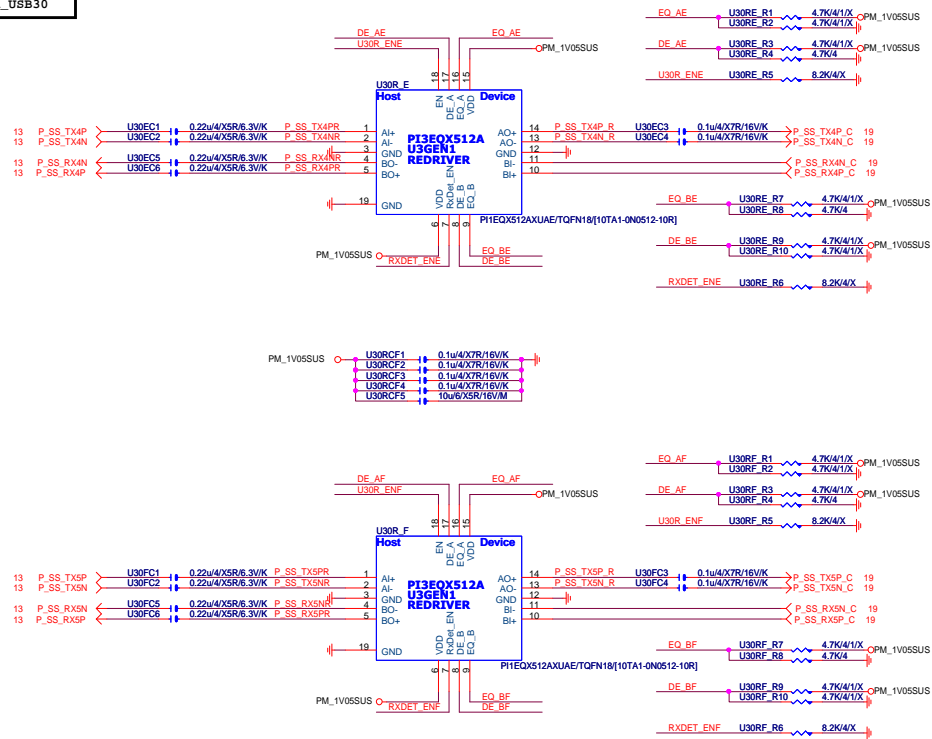
[I211]



F_USB30_1

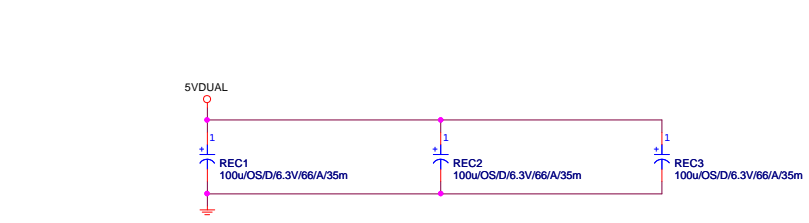
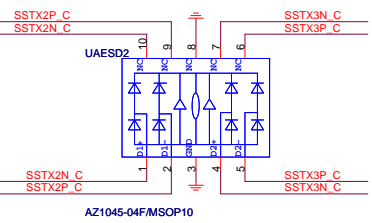
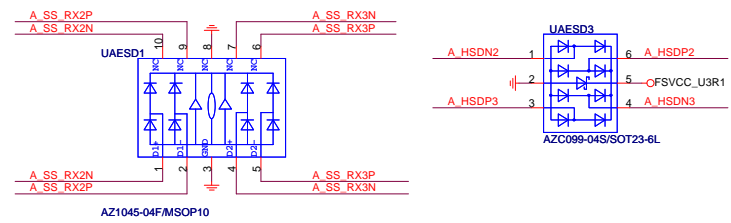
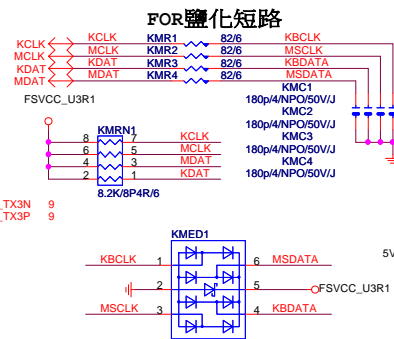
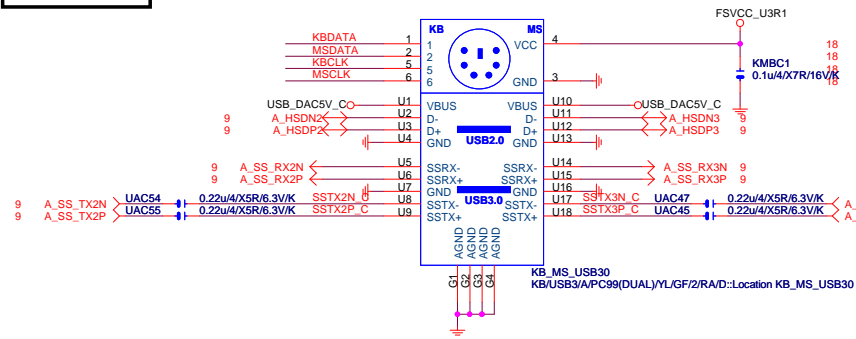
F_USB30_2

R_USB30

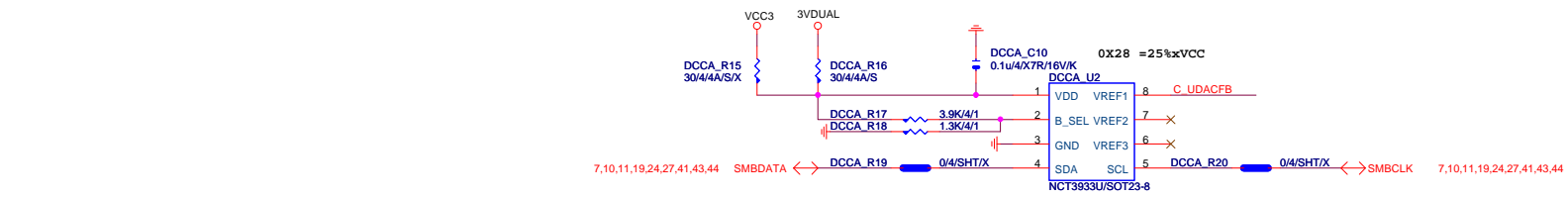
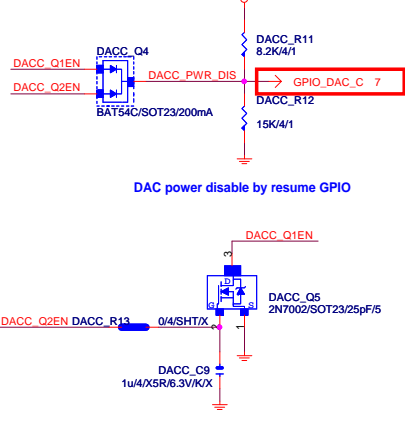
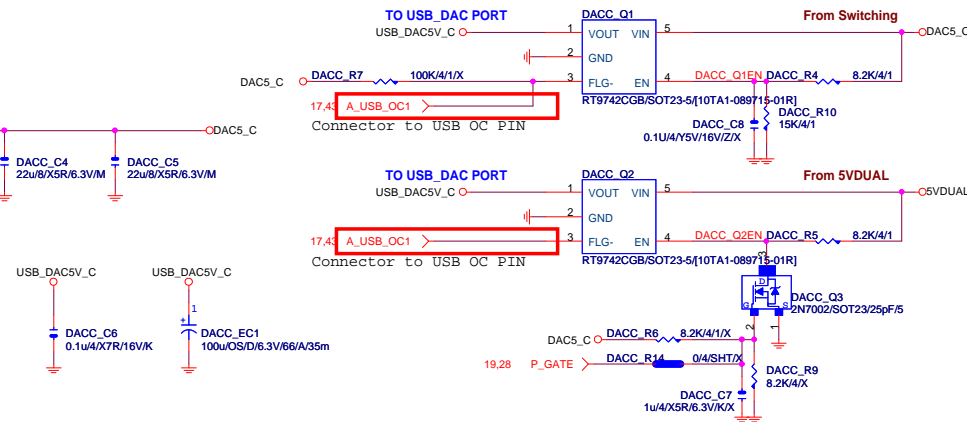
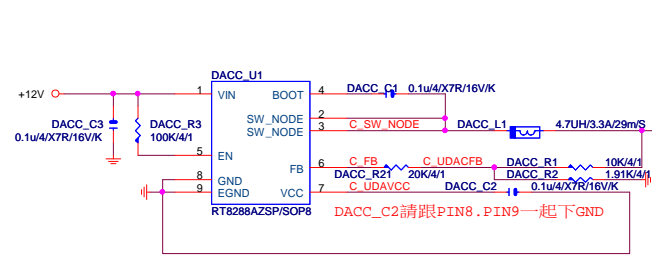
**GIGABYTE™**

Title			
PM_USB30_Redriver			
Size	Document Number	Rev	
C	GA-AX370-Gaming K5	1.01	
Date:	Tuesday, November 07, 2017	Sheet	30 of 44

KB/MS/DAC PWR

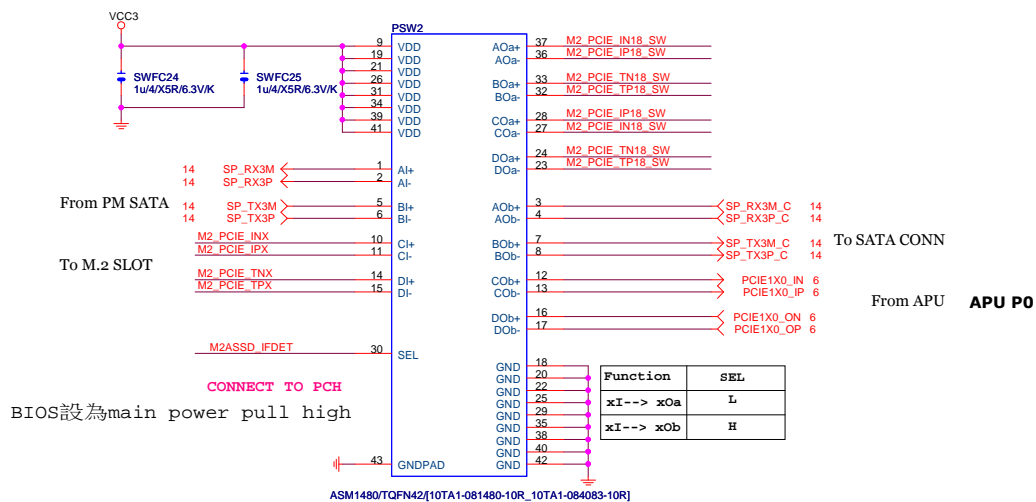
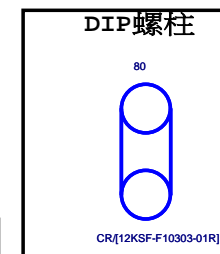
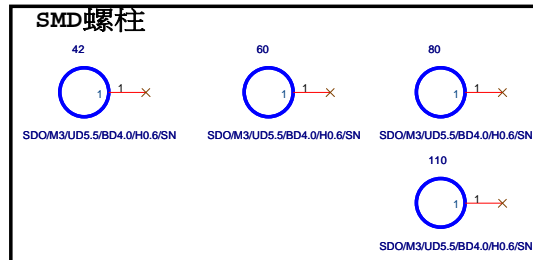
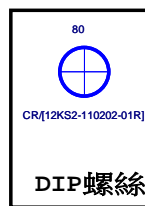
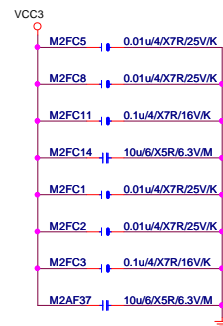
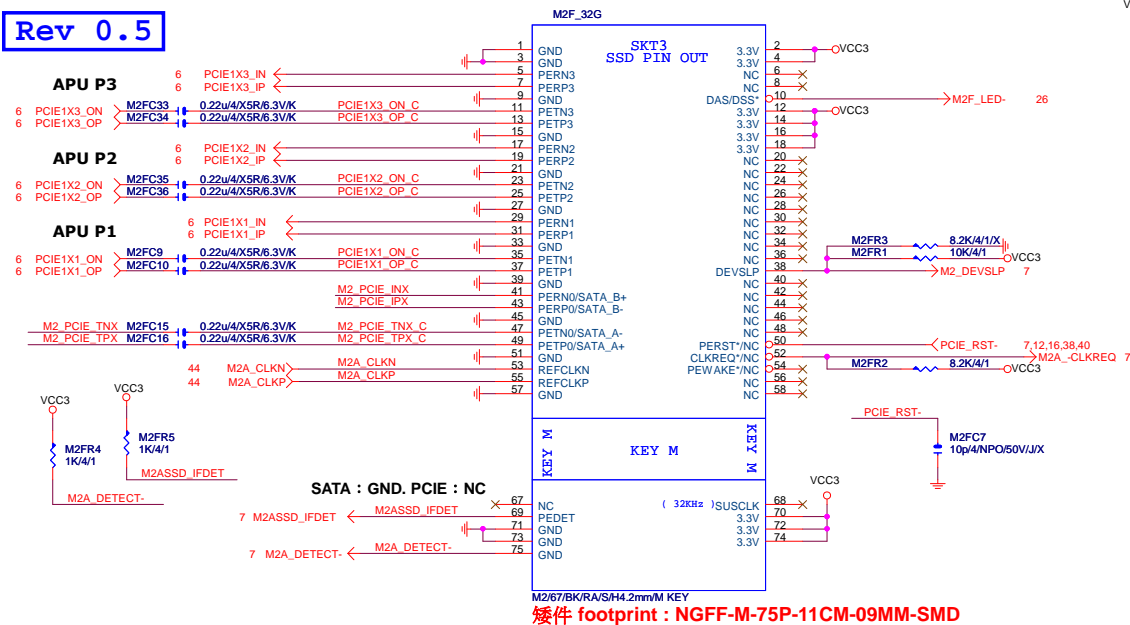


USB_DAC_C REV:0.13



GIGABYTE™		
Title KB_MS_USB30		
Size Custom	Document Number GA-AX370-Gaming K5	Rev 1.01
Date: Tuesday, November 07, 2017	Sheet 31	of 44

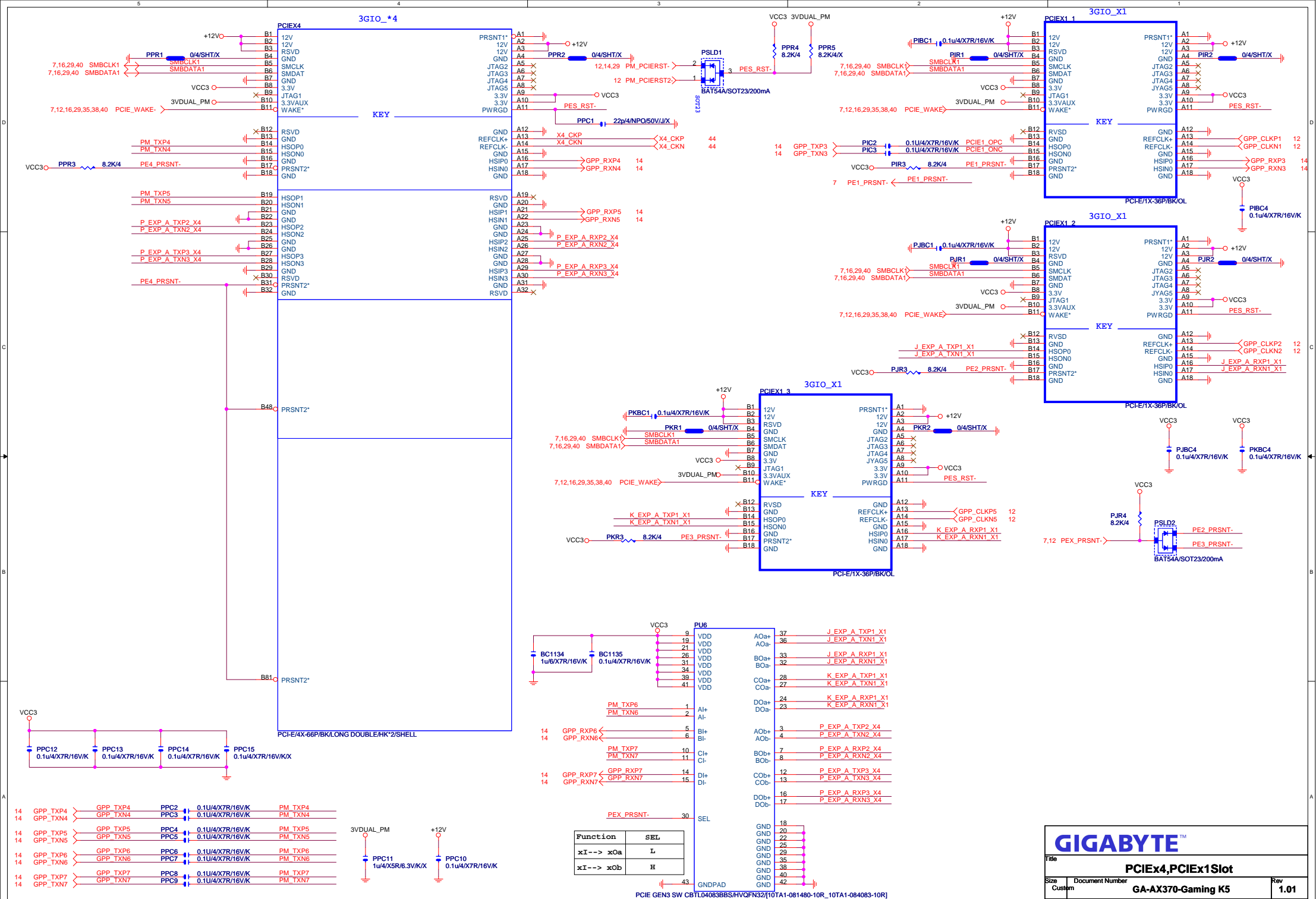
Rev 0.5

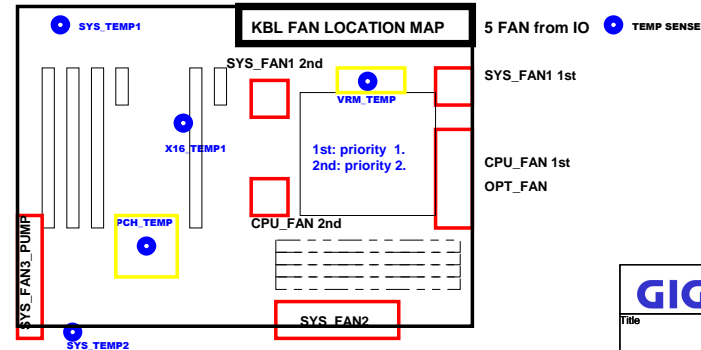


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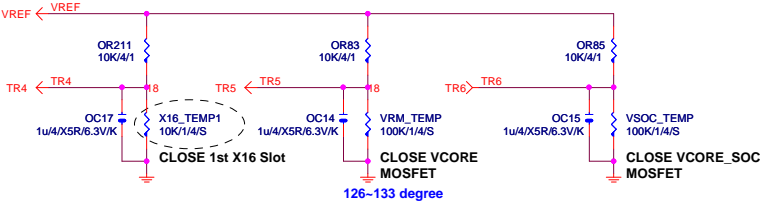
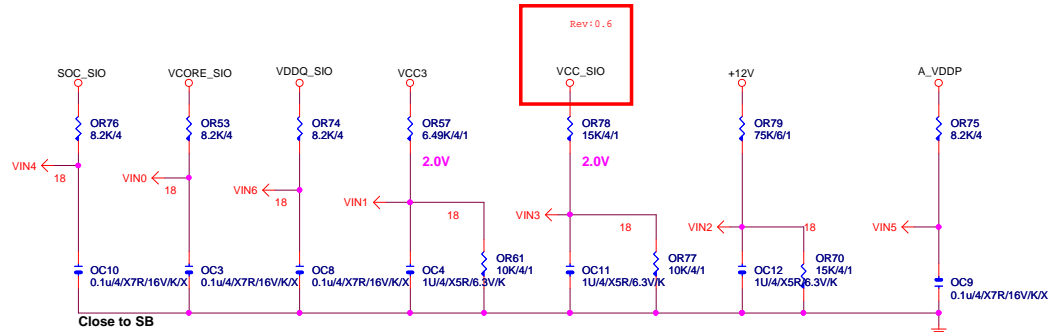
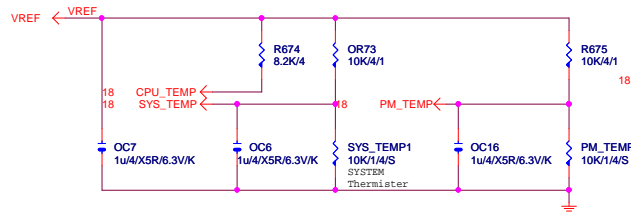
Title			M.2
Size	Document Number	Rev	1.01
Custom	GA-AX370-Gaming K5		
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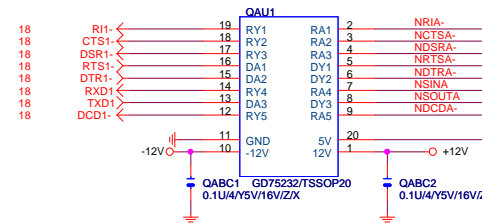


KBL FAN LOCATION MAP REFER TO PAGE.27

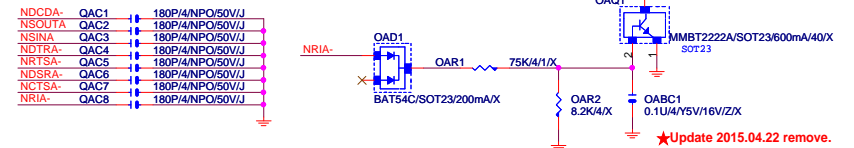
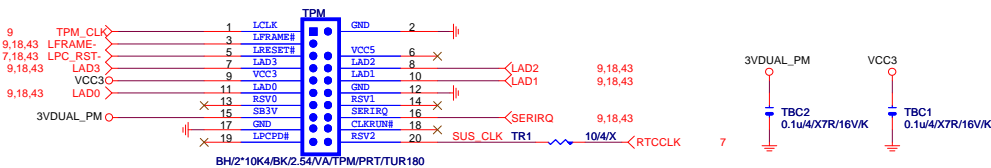
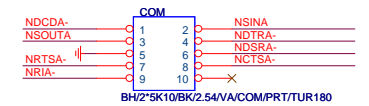
Hardware Monitor circuits



COM PORT



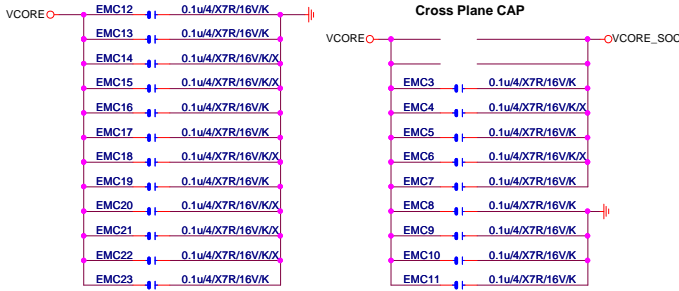
COMA



GIGABYTE

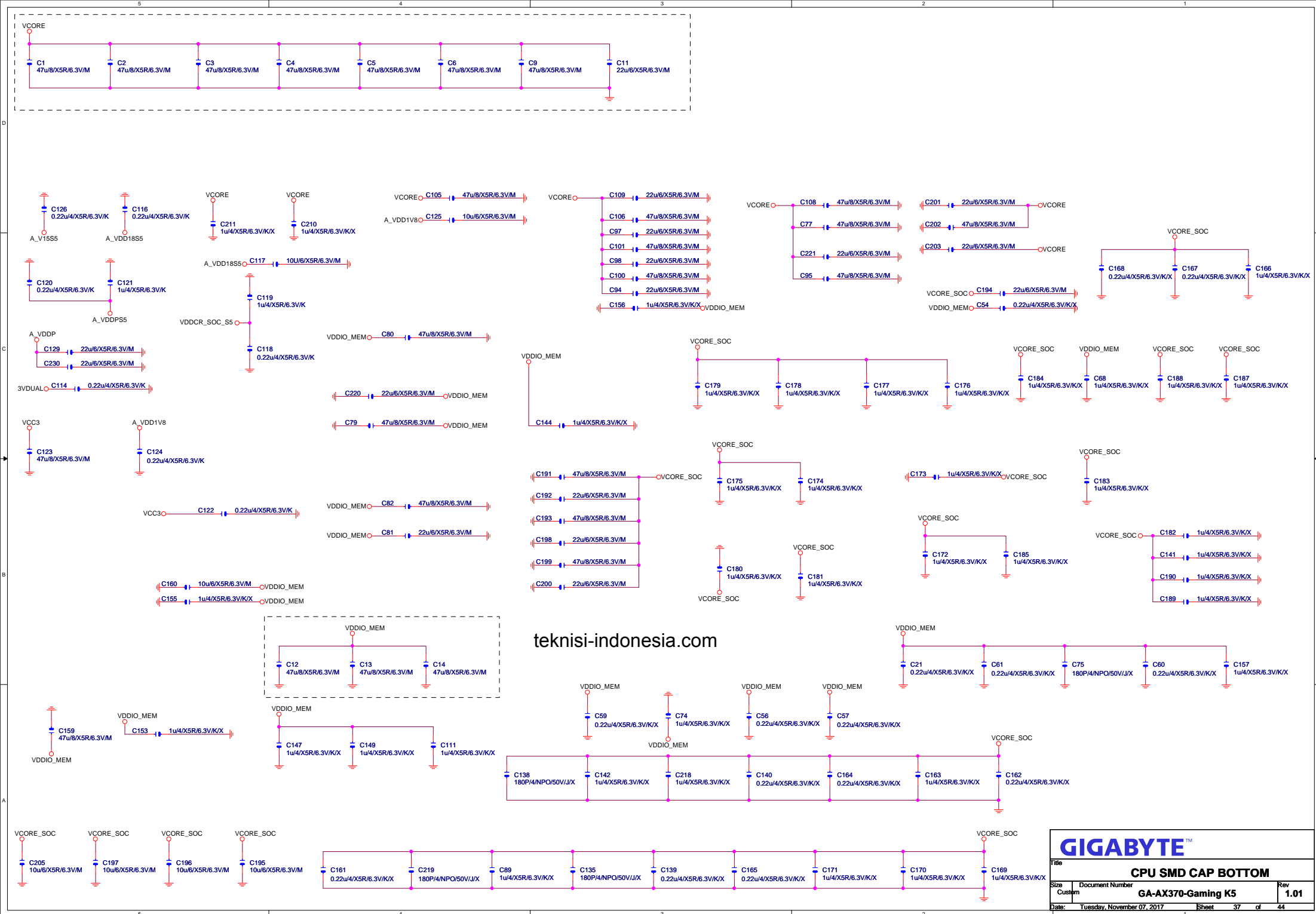
Title			HWM TPM, COM		
Size	Document Number	GA-AX370-Gaming K5			Rev
Custom					1.01
Date:	Tuesday, November 07, 2017	Sheet	35	of	44

CPU TOP CAVITY



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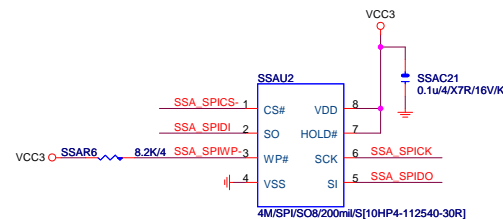
Title			
CPU SMD CAP TOP			
Size	Document Number	Rev	
Custom	GA-AX370-Gaming K5	1.01	
Date:	Tuesday, November 07, 2017	Sheet	36 of 44



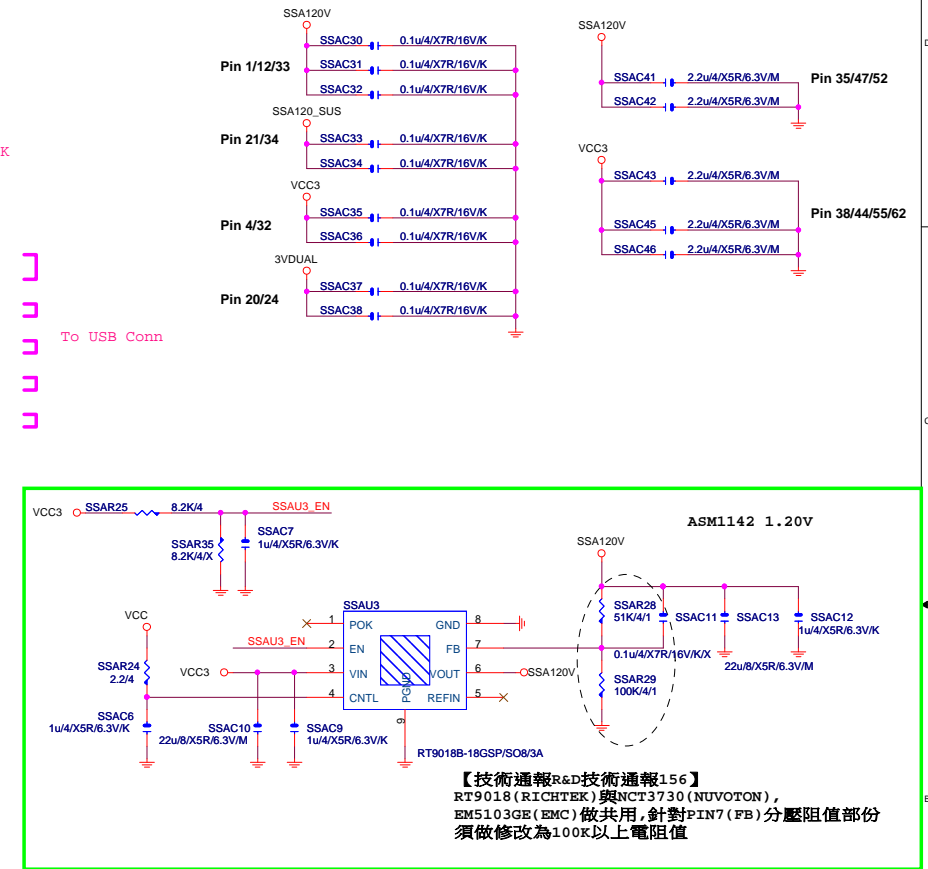
To PCIe host.

ASM1143 USB3.1

Base on ASM1142 0.3 Reference SCH

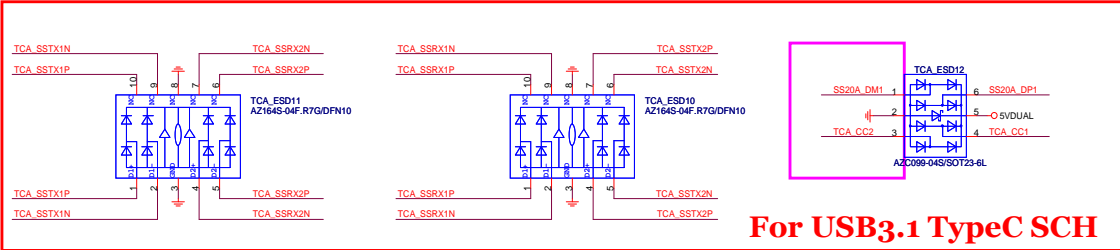
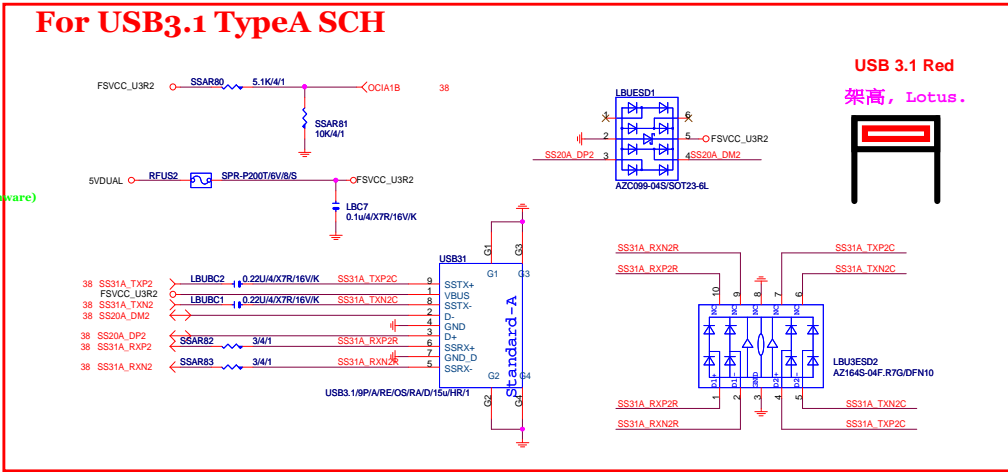
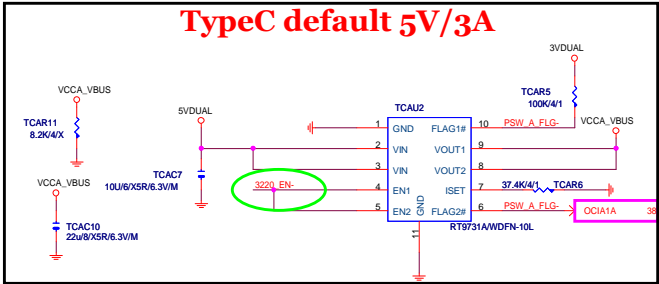
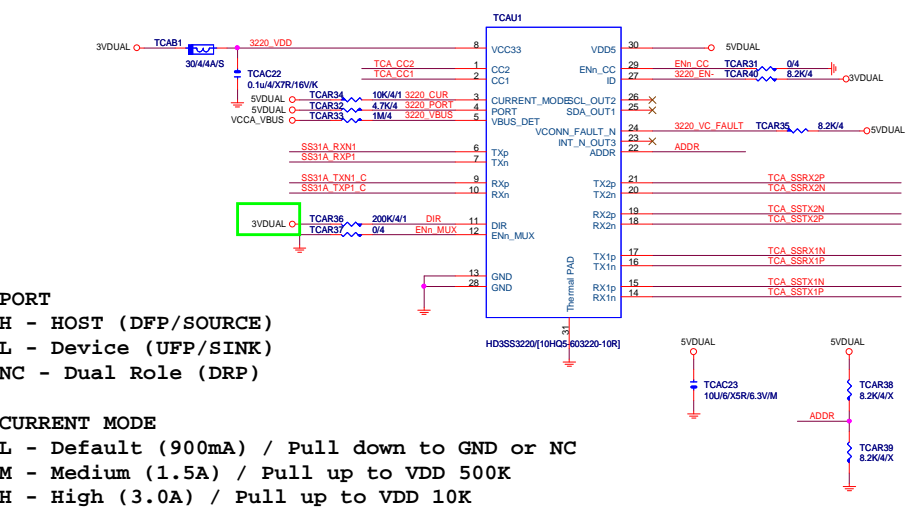
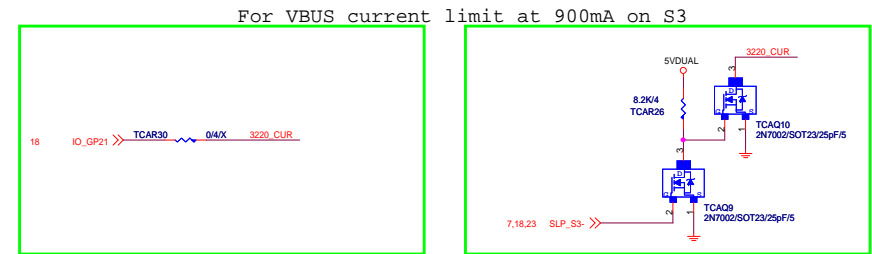
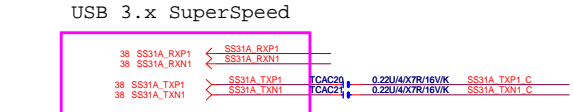


CSEL1	CSEL0	
1	1	External 20MHz Crystal (Asynchronous)
0	1	48MHz clock input (Synchronous)
X	0	Reserved for Test



【技術通報R&D技術通報156】
RT9018 (RICHTEK) 與 NCT3730 (NUVOTON),
EM5103GE (EMC) 做共用, 針對 PIN7 (FB) 分壓阻值部份
須做修改為 100K 以上電阻值

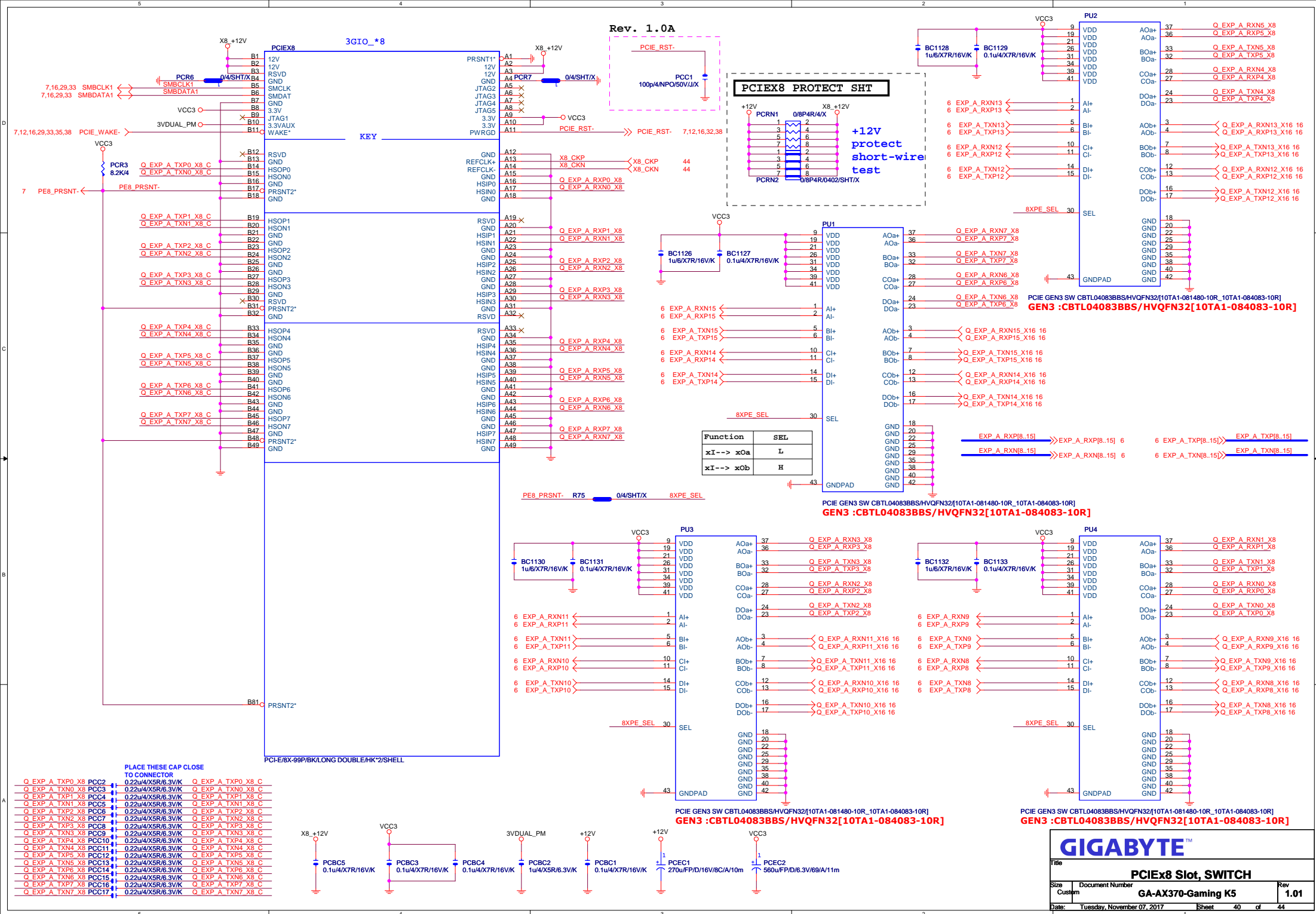
ASM2142 USB31 Host Rev0.3
TI HD3SS3220

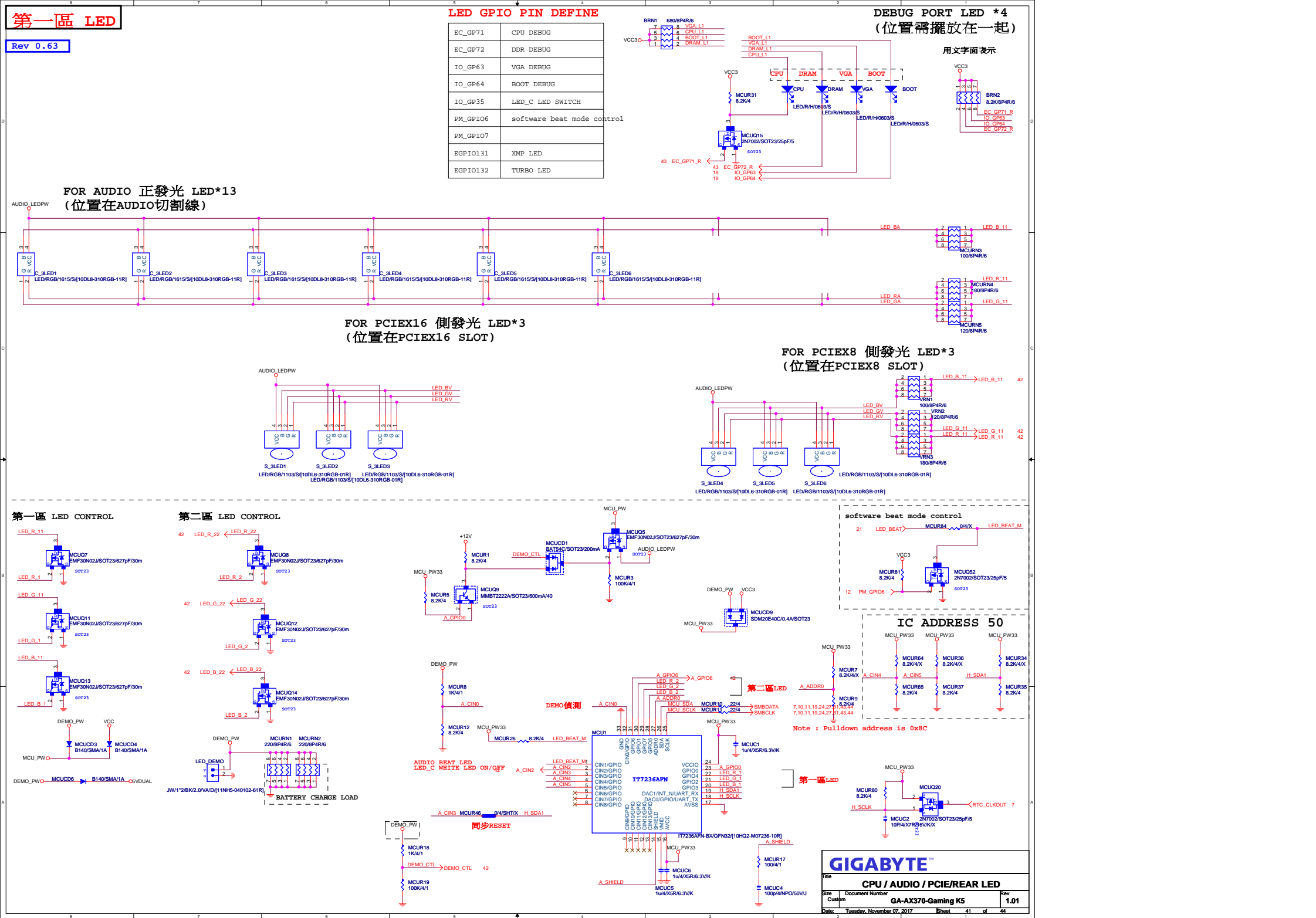


USB2.0 can be used the same source

Color markers can be changed by model

GIGABYTE™			
TI HD3SS3220			
Size C	Document Number	GA-AX370-Gaming K5	
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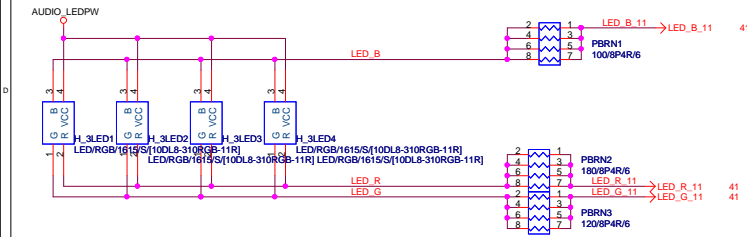




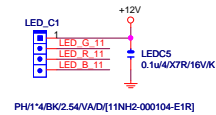
第二區 LED

Rev 0.63

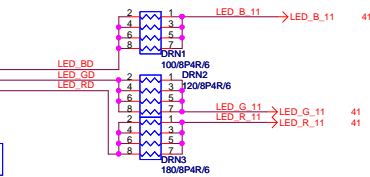
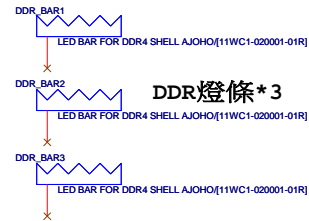
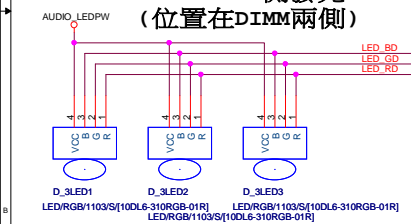
FOR PCH 正發光 LED*4 (依據PCH_HS設計擺放)



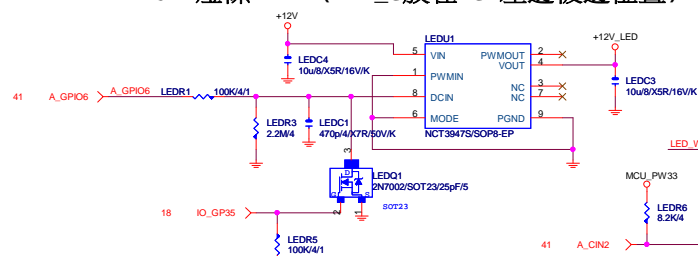
AMD CPU_FAN LED connector



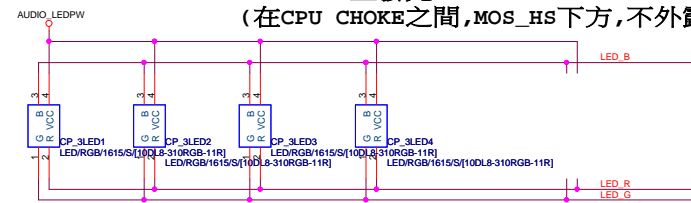
FOR DIMM 側發光 LED*6 (位置在DIMM兩側)



FOR 燈條 LED (LED_C放在PCB左邊板邊位置)

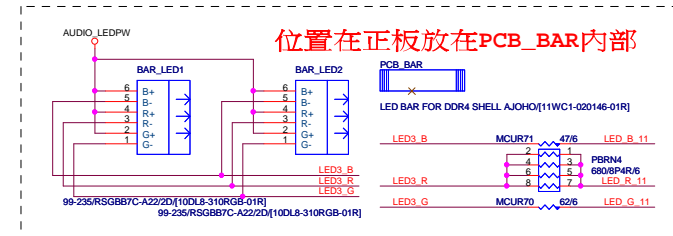


FOR CPU 正發光 LED*5 (在CPU CHOKE之間,MOS_HS下方,不外露)



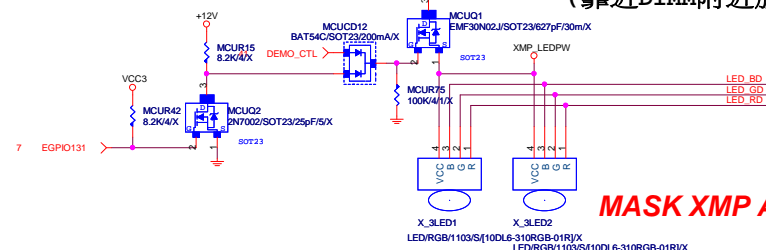
SC1M2/4.0mm/M1/0.5/3.5D[11KRH-010001-01R]

SC1M2/4.0mm/M1/0.5/3.5D[11KRH-010001-01R]



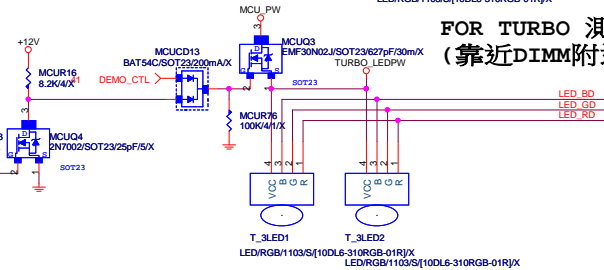
位置在正板放在PCB_BAR內部

FOR XMP 測發光 LED*2 (靠近DIMM附近放背板鏤空)



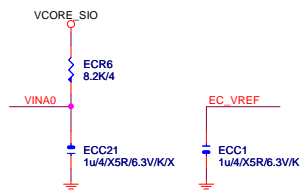
MASK XMP AND TURBO

FOR TURBO 測發光 LED*2 (靠近DIMM附近背板鏤空)

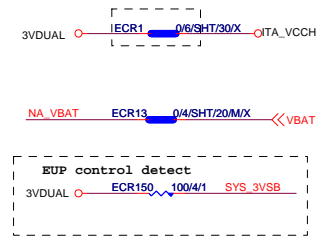
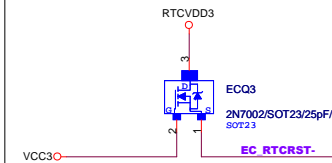


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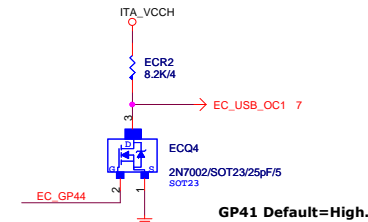
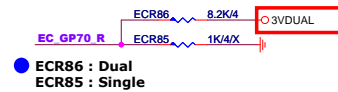
File	PCB / PCH / DDR / LED_C LED		
Size	Document Number	GA-AX370-Gaming K5	Rev 1.01
Custom			
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Watch Dog



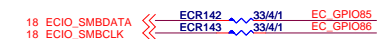
DUAL BIOS Strap



CORETYPE1(GP43)=Low(BR), EC_GP44 Default:Low, when GP41=Low, GP44=High.
CORETYPE1(GP43)=High(ST), EC_GP44 Default:High, when GP41=Low, GP44=Low.

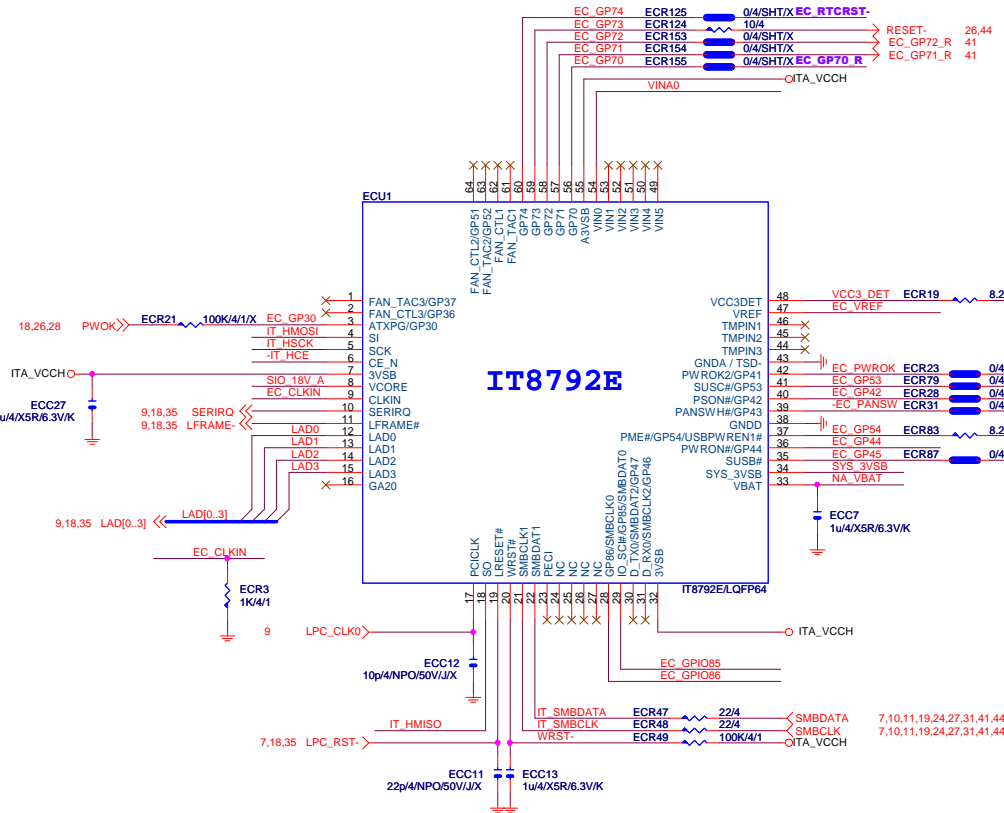
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IT8792 EC		
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internal power pin, max 22nF cap

